



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

This series is Cypress 32-bit microcontroller designed for automotive and industrial control applications. It contains the FR81S CPU that is compatible with the FR family. The FR81S has a high level performance among the Cypress FR family by enhancing CPU instruction pipeline and load store processing, and improving internal bus transfer.

It is best suited for application control for automotive.

Features

FR81S CPU Core

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Maximum operating frequency: 80 MHz (Source oscillation = 4.0 MHz and 20 multiplied (PLL clock multiplication system))
- General-purpose register: 32-bit x16 sets
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions appropriate to embedded applications
 - Memory-to-memory transfer instruction
 - Bit processing instruction
 - Barrel shift instruction etc.
- High-level language support instructions
 - Function entry/exit instructions
 - Register content multi-load and store instructions
- Bit search instructions
 - Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
 - Decrease overhead during branch process
- Register interlock function
 - Easy assembler writing
- Built-in multiplier and instruction level support
 - Signed 32-bit multiplication: 5 cycles
 - Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving)
 - 6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR family
- Built-in memory protection function (MPU)
 - Eight protection areas can be specified commonly for instructions and the data.
 - Control access privilege in both privilege mode and user mode.
- Built-in FPU (floating point arithmetic)
 - IEEE754 compliant
 - Floating-point register 32-bit x 16 sets

Peripheral Functions

- Clock generation (equipped with SSCG function)
 - Main oscillation (4 MHz)
 - Sub oscillation (32 kHz) or no sub oscillation
 - PLL multiplication rate: 1 to 20 times
- Built-in Program flash memory capacity
 - CY91F575: 512 + 64 KB
 - CY91F577: 1024 + 64 KB
 - CY91F578: 1536 + 64 KB
 - CY91F579: 2048 + 64 KB
- Built-in Data flash memory (WorkFlash) capacity 64 KB
- Built-in RAM capacity
 - Main RAM
 - CY91F575: 40 KB
 - CY91F577: 64 KB
 - CY91F578: 96 KB
 - CY91F579: 128 KB
 - Backup RAM
 - CY91F575/7: 8 KB
 - CY91F578/9: 16 KB
- General-purpose ports
 - [LQFP-144]**
 - 111 (none sub oscillation), 109 (with sub oscillation)
 - Included I²C pseudo open drain ports: 4
 - P057: Input only
 - [LQFP-208]**
 - 159 (none sub oscillation), 157 (with sub oscillation)
 - Included I²C pseudo open drain ports: 4
 - P057: Input only
- External bus interface
 - 22-bit address, 16-bit data
 - 23 pins of 9-bit address, 8-bit data, ASX, CS0X, CS1X, RDX, WR0X, and WR1X can select 5V/3.3V by the VCCE power supply
- DMA Controller
 - Up to 16 channels can be started simultaneously.
 - 2 transfer factors (Internal peripheral request and software)

- A/D converter (successive approximation type)
 - 8/10-bit resolution: 40 channels
 - Conversion time: 3 μ s
- D/A converter (R-2R type)
 - 8-bit resolution: 2 channels
- External interrupt input: 16 channels
 - Level ("H" / "L"), or edge detection (rising or falling) enabled
- LIN-UART
 - 6 channels, ch.2 to ch.7
 - Selectable from UART, synchronous mode or LIN-UART mode
 - LIN protocol Revision 2.1 supported (LIN-UART).
 - SPI (Serial Peripheral Interface) supported (synchronous mode)
 - Full-duplex double buffering system
 - LIN synch break detection (linked to the input capture)
 - Built-in dedicated baud rate generator
 - DMA transfer support
- Multi-function serial communication (built-in transmission/reception FIFO memory): 4 channels

< UART (Asynchronous serial interface) >

- Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
- Parity or no parity is selectable.
- Built-in dedicated baud rate generator
- The external clock can be used as the transfer clock
- Parity, frame, and overrun error detect functions provided
- DMA transfer support

< CSIO (Synchronous serial interface) >

- Full-duplex double buffering system, 16-byte transmission FIFO, memory, 16-byte reception FIFO memory
- SPI supported; master and slave systems supported; 5 to 9-bit data length can be set.
- Built-in dedicated baud rate generator (Master operation)
- The external clock can be entered. (Slave operation)
- Overrun error detection function is provided
- DMA transfer support

< LIN-UART (Asynchronous Serial Interface for LIN) >

- Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
- LIN protocol revision 2.1 supported
- Master and slave systems supported
- Framing error and overrun error detection
- LIN synch break generation and detection; LIN synch delimiter generation
- Built-in dedicated baud rate generator
- The external clock can be adjusted by the reload counter
- DMA transfer support

< I²C >

- Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
- Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported
- DMA transfer supported (for transmission only)
- I²C supporting I/O (for ch.0 and ch.1 only)
- CAN Controller (C-CAN): 3 channels
 - Transfer speed: Up to 1 Mbps
 - 64-transmission/reception message buffering: 1 channel, 32-transmission/reception message buffering: 2 channels
- PPG: 16-bit \times 24 channels
- Reload timer: 16-bit \times 7 channels (3 channels are for regular timer interrupt generation.)
- Free-run timer:
 - 32-bit \times 6 channels (Can select each channel for input capture, output compare)
- Input capture:
 - 32-bit \times 12 channels (linked to the free-run timer)
- Output compare: 32-bit \times 12 channels (linked to the free-run timer)
- Sound generator: 5 channels
 - Frequency and amplitude sequencers provided
- Stepping motor controller: 6 channels
 - 8/10-bit PWM
 - High current output supported (4 lines \times 6 channels)
 - Can refer back electromotive force using pin-shared A/D converter
- LCD controller
 - Common output: 4, Segment output: 32
 - Duty drive (SEG0 to SEG31) and static drive (ST0 to ST8) can be switched.
 - Each of COM0 to COM3, SEG0 to SEG31, V0, V1, V2, and V3 pins for duty drive can be switched to the general-purpose port. (The SEG23 to SEG31 pins can be switched to static driving.)
 - V0, V1, V2 and V3 pin can be used as the general-purpose port. But V3 pin cannot be used as an output pin.
 - Each of ST0 to ST8 pins for static drive can be switched to the general-purpose port, or it can be switched to the segment output of duty drive.
 - CY91F575/7: The amplitude of the SEG0 to SEG22 output is determined by the VCC5 power supply pin or by the V3 pin even if VCCE pin is supplied to 3.3 V.
 - CY91F578/9: The voltage VCCE or less can be supplied to V3 pin. It is prohibited that VCC5 being chosen as LCDC reference voltage by software.
- Up/Down counter: 2 channels
 - 8/16-bit up/down counter
- Real-time clock (RTC) (for day, hours, minutes, seconds)
 - Main oscillation / sub oscillation frequency can be selected for the operation clock

- Calibration: A hardware watchdog of the CR oscillation drive and real-time clock (RTC) of the sub clock drive
 - The CR oscillation frequency can be trimmed
 - The main clock to sub clock ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
 - Monitoring abnormality (damage of crystal etc.) of sub oscillation (32 kHz) (dual clock products) and main oscillation (4 MHz)
 - When abnormality is detected, it switches to the CR clock.
- Base timer: 2 channels
 - 16-bit timer
 - Any of four PWM/PPG/PWC/reload timer functions can be selected and used.
 - As for the functions of PWC and reload timer, 2 channels of cascade mode can be used as 32-bit timer.
- CRC generation
- HS-SPI
 - Note:** In this series, the HS-SPI function is prohibited
 - E²PROM and the flash device of the Single/Dual/Quad-SPI protocol can be connected.
 - The power supply of 5V/3.3V supplied to the VCCE power supply pin is used.
 - Maximum 16 MHz (Maximum 8 MHz at the slave.)
- Watchdog timer
 - Hardware watchdog
 - Software watchdog
- NMI
- Interrupt controller
- Interrupt request batch read
 - Multiple interrupts from peripherals can be read by a series of registers.
- I/O relocation
 - Peripheral function pins can be reassigned.
- Low-power consumption mode
 - Sleep / Stop / Watch / Sub RUN mode
 - Stop (power shutdown) / Watch (power shutdown) mode
- Power on reset
- Low-voltage detection reset (external low-voltage detection)
- Low-voltage detection reset (internal low-voltage detection)
- Device Package:
 - LQFP-144 for CY91F575/7/8/9
 - LQFP-208 for CY91F578/9
- CMOS 90nm Technology
- Power supplies
 - 5V Power supply
 - The internal 1.2 V is generated from 5 V with the voltage step-down regulator.
 - I/O port uses the power supply of 5V/3.3V supplied to the VCCE power supply pin.
 - LQFP-144: P010 to P017, P020 to P027, and P030 to P036
 - LQFP-208: P140 to P147, P150 to P157, P160 to P167, P170 to P177, P180 to P187, and P190 to P197

Contents

1. Product Lineup..... 5

2. Pin Assignment (LQFP-144)..... 11

3. Pin Assignment (LQFP-208)..... 12

4. Pin Description (LQFP-144)..... 13

5. Pin Description (LQFP-208)..... 29

6. I/O Circuit Type..... 43

7. Handling Precautions 49

7.1 Precautions for Product Design..... 49

7.2 Precautions for Package Mounting..... 50

7.3 Precautions for Use Environment..... 51

8. Handling Devices 52

9. Block Diagram 55

10. Memory Map 56

11. I/O Map 60

12. Interrupt Vector Table..... 101

13. Electrical Characteristics 104

13.1 Absolute Maximum Ratings..... 104

13.2 Recommended Operating Conditions..... 106

13.3 DC Characteristics..... 107

13.4 AC Characteristics..... 114

13.5 A/D Converter..... 150

13.6 D/A Converter..... 153

13.7 Flash Memory..... 154

14. Ordering Information 155

15. Package Dimensions 156

16. Major Changes 159

Document History..... 160

Sales, Solutions, and Legal Information..... 161

1. Product Lineup

Item	Product	CY91F575B(S)/C(S)	CY91F575BH(S)/CH(S)
System Clock		On chip PLL Clock multiple method	
Minimum instruction execution time		Around 12.5 ns (80 MHz)	
Sub clock		Yes (Non-S series) No (S series)	
FLASH Capacity (Program)		512 + 64 KB	
FLASH Capacity (Work)		64 KB	
RAM		40 KB + 8 KB	
BI-ROM		4 KB	
GDC		None	
External BUS I/F		Address: 22-bit Data:16-bit (Part of the External BUS I/F pins can select the power supply 5 V or 3.3 V)	
DMA Controller		16 channels	
Base Timer(16-bit)		2 channels	
Free-run Timer(32-bit)		6 channels	
Input capture(32-bit)		12 channels	
Output Compare(32-bit)		12 channels	
Reload Timer(16-bit)		7 channels	
PPG timer(16-bit)		24 channels	
Up/down Counter		2 channels	
Clock Supervisor		Yes	
D/A converter		2 channels	
External Interrupt		16 channels	
A/D converter (8-bit/10-bit)		40 channels	
LIN-UART		6 channels	
Multi-Function serial communication		4 channels ^{**1}	
HS-SPI		Yes Up to 16 MHz Note: In this series, the HS-SPI function is prohibited.	
LCD Controller		32 seg × 4 com (Static drive 8seg × 1com)	
CAN		64 msg × 1 channel / 32 msg × 2 channels	
Stepping Motor Controller		6 channels	

Item	Product	CY91F575B(S)/C(S)	CY91F575BH(S)/CH(S)
	Sound Generator	5 channels	
Software Watchdog	Yes		
Hardware Watchdog	Yes		
Clock supervisor	Initial value "ON"	Initial value "OFF"	
CRC generation	Yes		
Low-voltage detection reset (External low-voltage detection)	Yes		
Low-voltage detection reset (Internal low-voltage detection)	Yes		
Package	LQFP-144		
Others	Flash Products		
On Chip Debug	Yes		

*1: I²C only supported by ch.0 and ch.1.

Item	Product	CY91F577B(S)/C(S)	CY91F577BH(S)/CH(S)
System Clock		On chip PLL Clock multiple method	
Minimum instruction execution time		Around 12.5 ns (80 MHz)	
Sub clock		Yes (Non-S series) No (S series)	
FLASH Capacity (Program)		1024 + 64 KB	
FLASH Capacity (Work)		64 KB	
RAM		64 KB + 8 KB	
BI-ROM		4 KB	
GDC		None	
External BUS I/F		Address: 22-bit Data:16-bit (Part of the External BUS I/F pins can select the power supply 5 V or 3.3 V)	
DMA Controller		16 channels	
Base Timer(16-bit)		2 channels	
Free-run Timer(32-bit)		6 channels	
Input capture(32-bit)		12 channels	
Output Compare(32-bit)		12 channels	
Reload Timer(16-bit)		7 channels	
PPG timer(16-bit)		24 channels	
Up/down Counter		2 channels	
Clock Supervisor		Yes	
D/A converter		2 channels	
External Interrupt		16 channels	
A/D converter (8-bit/10-bit)		40 channels	
LIN-UART		6 channels	
Multi-Function serial communication		4 channels ^{*1}	
HS-SPI		Yes Up to 16 MHz Note: In this series, the HS-SPI function is prohibited.	
LCD Controller		32 seg × 4 com (Static drive 8 seg × 1com)	
CAN		64 msg × 1 channel / 32 msg × 2 channels	
Stepping Motor Controller		6 channels	
Sound Generator		5 channels	

Item	Product	CY91F577B(S)/C(S)	CY91F577BH(S)/CH(S)
Software Watchdog	Yes		
Hardware Watchdog	Yes		
Clock supervisor	Initial value "ON"	Initial value "OFF"	
CRC generation	Yes		
Low-voltage detection reset (External low-voltage detection)	Yes		
Low-voltage detection reset (Internal low-voltage detection)	Yes		
Package	LQFP-144		
Others	Flash Products		
On Chip Debug	Yes		

*1: I²C only supported by ch.0 and ch.1.

Item	Product	CY91F 578C(S)(M)	CY91F 578CH(S)(M)	CY91F 579C(S)(M)	CY91F 579CH(S)(M)
System Clock		On chip PLL Clock multiple method			
Minimum instruction execution time		Around 12.5 ns (80 MHz)			
Sub clock		Yes (Non-S series) No (S series)			
FLASH Capacity (Program)		1536 + 64 KB		2048 + 64 KB	
FLASH Capacity (Work)		64 KB			
RAM		96 KB + 16 KB		128 KB + 16 KB	
BI-ROM		4 KB			
GDC		None			
External BUS I/F		Address: 22-bit Data:16-bit (Part of the External BUS I/F pins can select the power supply 5 V or 3.3 V)			
DMA Controller		16 channels			
Base Timer(16-bit)		2 channels			
Free-run Timer(32-bit)		6 channels			
Input capture(32-bit)		12 channels			
Output Compare(32-bit)		12 channels			
Reload Timer(16-bit)		7 channels			
PPG timer(16-bit)		24 channels			
Up/down Counter		2 channels			
Clock Supervisor		Yes			
D/A converter		2 channels			
External Interrupt		16 channels			
A/D converter (8-bit/10-bit)		40 channels			
LIN-UART		6 channels			
Multi-Function serial communication		4 channels ^{*1}			
HS-SPI		No			
LCD Controller		32 seg × 4 com (Static drive 8 seg × 1 com)			
CAN		64 msg × 1 channel / 32 msg × 2 channels			
Stepping Motor Controller		6 channels			
Sound Generator		5 channels			
Software Watchdog		Yes			

Item	Product	CY91F 578C(S)(M)	CY91F 578CH(S)(M)	CY91F 579C(S)(M)	CY91F 579CH(S)(M)
Hardware Watchdog	Yes				
Clock supervisor	Initial value "ON"	Initial value "OFF"	Initial value "ON"	Initial value "OFF"	
CRC generation	Yes				
Low-voltage detection reset (External low-voltage detection)	Yes				
Low-voltage detection reset (Internal low-voltage detection)	Yes				
Package	LQFP-144 LQFP-208 (with suffix "M")				
Others	Flash Products				
On Chip Debug	Yes				

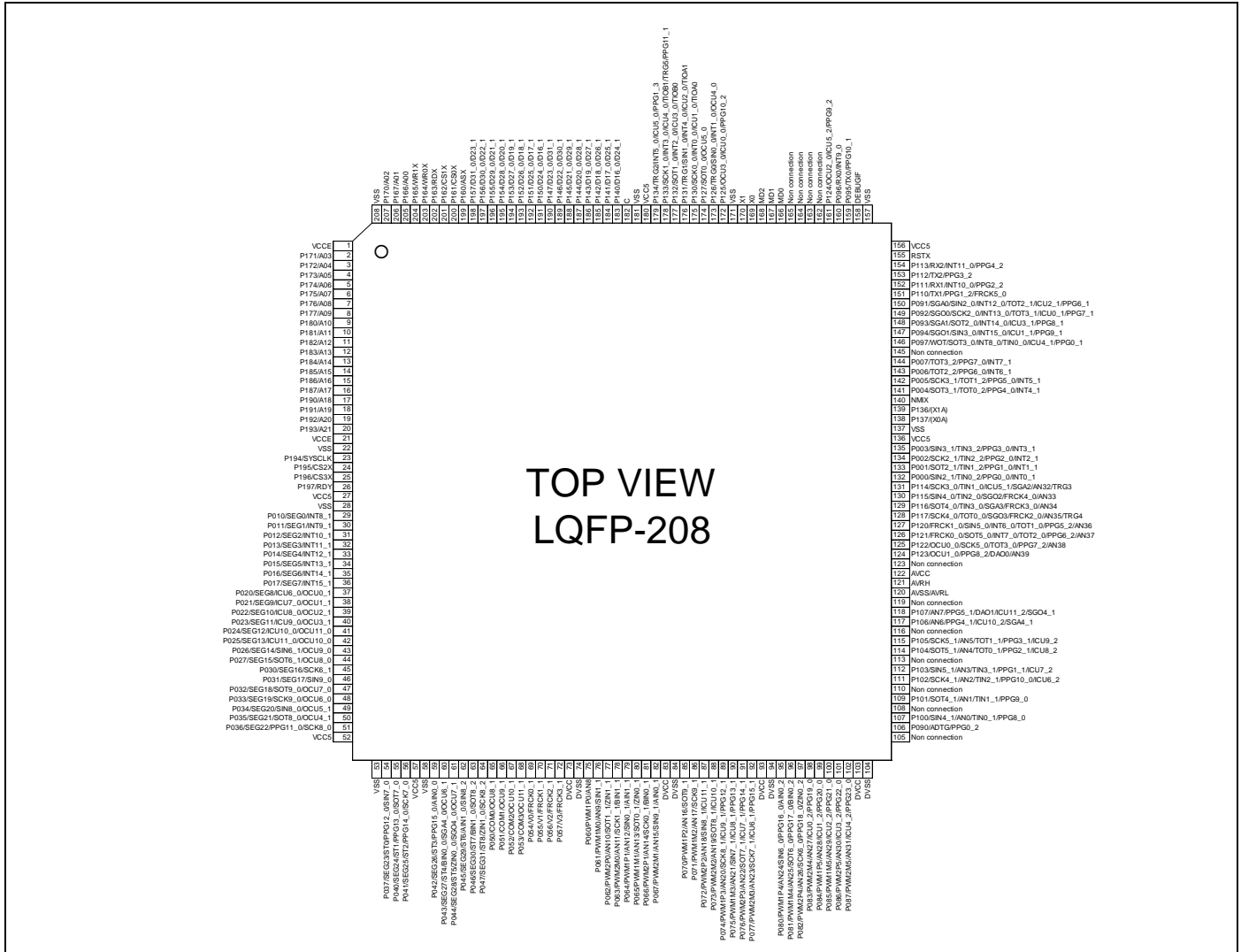
*1: I²C only supported by ch.0 and ch.1.

2. Pin Assignment (LQFP-144)

Pin 1-36		Pin 37-72		Pin 73-109	
1	VCCE	37	VSS	108	VCC5
2	P015/D29_0/SEG5/D21_1/INT13_1	38	P055/CS2X/1/FRCK1_1	107	RSTX
3	P016/D30_0/SEG6/D22_1/INT14_1	39	P056/CS3X/2/FRCK2_1	106	P113/RX2/INT11_0/PPG4_2
4	P017/D31_0/SEG7/D23_1/INT15_1	40	P057/RDY/3/FRCK3_1	105	P112/TX2/PPG3_2
5	P020/ASX/SEG8/ICU6_0/OCU0_1	41	DVCC 41	104	P111/RX1/INT10_0/PPG2_2
6	P021/CS0X/SEG9/ICU7_0/OCU1_1	42	DVSS 42	103	P110/TX1/PPG1_2/FRCK5_0
7	P022/CS1X/SEG10/ICU8_0/OCU2_1	43	P060/PWM1/P0AN8	102	P091/SGA0/SIN2_0/INT12_0/TOT2_1/ICU2_1/PPG6_1
8	P023/RDX/SEG11/ICU9_0/OCU3_1	44	P061/PWM1/M0AN9/SIN1_1	101	P092/SGO0/SCK2_0/INT13_0/TOT3_1/ICU0_1/PPG7_1
9	P024/WR0X/SEG12/ICU10_0/OCU11_0	45	P062/PWM2/P0/AN10ZIN1_1/SOT1_1	100	P093/SGA1/SOT2_0/INT14_0/ICU3_1/PPG8_1
10	P025/WR1X/SEG13/ICU11_0/OCU10_0	46	P063/PWM2/M0/AN11BINT_1/SOT1_1	99	P094/SGO1/SIN3_0/INT15_0/ICU1_1/PPG9_1
11	P026/A00/SEG14/SPL_CS3/SIN6_1/OCU9_0	47	P064/PWM1/P1/AN12ZAIN1_1/SIN0_1	98	P097/WOT/SOT3_0/INT8_0/TIN0_0/ICU4_1/PPG0_1
12	P027/A01/SEG15/SPL_CS2/SOT6_1/OCU8_0	48	P065/PWM1/M1/AN13ZINO_1/SOT0_1	97	NMIX
13	P030/A02/SEG16/SPL_CS1/SCK6_1	49	P066/PWM2/P1/AN14BIN0_1/SCK0_1	96	P136/(X1A)
14	P031/A03/SEG17/SPL_CS0/SIN9_0	50	P067/PWM2/M1/AN15AIN0_1/SIN9_1	95	P137/(X0A)
15	P032/A04/SEG18/SPL_SIO3/SOT9_0/OCU7_0	51	DVCC 51	94	VSS
16	P033/A05/SEG19/SPL_SIO2/SCK9_0/OCU6_0	52	DVSS 52	93	VCC5
17	P034/A06/SEG20/SPL_SIO1/SIN8_0/OCU5_1	53	P070/PWM1/P2/AN16/SOT9_1	92	P114/SCK3_0/TIN1_0/ICU5_1/SGA2/TRG3/AN32
18	P035/A07/SEG21/SPL_SIO0/SOT8_0/OCU4_1	54	P071/PWM1/M2/AN17/SCK9_1	91	P115/SIN4_0/TIN2_0/SGO2/FRCK4_0/AN33
19	P036/A08/SEG22/PPG11_0/SPL_CLK/SCK8_0	55	P072/PWM2/P2/AN18/ICU11_1/SIN8_1	90	P118/SOT4_0/TIN3_0/SGA3/FRCK3_0/AN34
20	VCCE	56	P073/PWM2/M2/AN19/ICU10_1/SOT8_1	89	P117/SCK4_0/TOT0_0/SGO3/TRG4/FRCK2_0/AN35
21	VSS	57	P074/PWM1/P3/AN20/PPG12_1/ICU9_1/SCK8_1	88	P120/FRCK1_0/SIN5_0/INT6_0/TOT1_0/PPG5_2/AN36
22	P037/A09/SEG23/ST0/PPG12_0/SIN7_0	58	P075/PWM1/M3/AN21/PPG13_1/ICU8_1/SIN7_1	87	P121/FRCK0_0/SOT5_0/INT7_0/TOT2_0/PPG6_2/AN37
23	P040/A10/SEG24/ST1/PPG13_0/SOT7_0	59	P076/PWM2/P3/AN22/PPG14_1/ICU7_1/SOT7_1	86	P122/OCU0_0/SCK5_0/TOT3_0/PPG7_2/AN38
24	P041/A11/SEG25/ST2/PPG14_0/SCK7_0	60	P077/PWM2/M3/AN23/PPG15_1/ICU6_1/SCK7_1	85	P123/OCU1_0/PPG8_2/DAO0/AN39
25	P042/A12/SEG26/ST3/PPG15_0/AIN0_0	61	DVCC 61	84	AVCC
26	P043/A13/SEG27/ST4/BIN0_0/SGA4_0/OCU6_1	62	DVSS 62	83	AVRH
27	P044/A14/SEG28/ST5/ZINO_0/SGO4_0/OCU7_1	63	P080/PWM1/P4/AN24/SIN6_0/PPG16_0/AIN0_2	82	AVSS/AVRL
28	P046/A15/SEG29/ST6/AIN1_0/SIN8_2	64	P081/PWM1/M4/AN25/SOT6_0/PPG17_0/BIN0_2	81	P107/AN7/PPG5_1/DAO1/ICU11_2/SGO4_1
29	P046/A16/SEG30/ST7/BIN1_0/SOT8_2	65	P082/PWM2/P4/AN26/SCK6_0/PPG18_0/ZINO_2	80	P106/AN6/PPG4_1/ICU10_2/SGA4_1
30	P047/A17/SEG31/ST8/ZIN1_0/SCK8_2	66	P083/PWM2/M4/AN27/ICU11_2/PPG19_0	79	P105/SCK5_1/AN5/TOT1_1/PPG3_1/ICU9_2
31	P050/A18/COM0/OCU8_1	67	P084/PWM1/P5/AN28/ICU11_2/PPG20_0	78	P104/SOT5_1/AN4/TOT0_1/PPG2_1/ICU8_2
32	P051/A19/COM1/OCU9_1	68	P085/PWM1/M5/AN29/ICU2_2/PPG21_0	77	P103/SIN5_1/AN3/TIN3_1/PPG1_1/ICU7_2
33	P052/A20/COM2/OCU10_1	69	P086/PWM2/P5/AN30/ICU3_2/PPG22_0	76	P102/SCK4_1/AN2/TIN2_1/PPG10_0/ICU6_2
34	P053/A21/COM3/OCU11_1	70	P087/PWM2/M5/AN31/ICU4_2/PPG23_0	75	P101/SOT4_1/AN1/TIN1_1/PPG9_0
35	P054/SYSCLK/V0/FRCK0_1	71	DVCC 71	74	P100/SIN4_1/AN0/TIN0_1/PPG8_0
36	VCC5	72	DVSS 72	73	P090/ADTG/PPG0_2
144	VSS				
143	P014/D28_0/SEG4/D20_1/INT12_1				
142	P013/D27_0/SEG3/D19_1/INT11_1				
141	P012/D26_0/SEG2/D18_1/INT10_1				
140	P011/D25_0/SEG1/D17_1/INT9_1				
139	P010/D24_0/SEG0/D16_1/INT8_1				
138	P007/D23_0/TOT3_2/PPG7_0/D31_1/INT7_1				
137	P006/D22_0/TOT2_2/PPG6_0/D30_1/INT6_1				
136	P005/D21_0/SCK3_1/TOT1_2/PPG5_0/D29_1/INT5_1				
135	P004/D20_0/SOT3_1/TOT0_2/PPG4_0/D28_1/INT4_1				
134	P003/D19_0/SIN3_1/TIN3_2/PPG3_0/D27_1/INT3_1				
133	P002/D18_0/SCK2_1/TIN2_2/PPG2_0/D26_1/INT2_1				
132	P001/D17_0/SOT2_1/TIN1_2/PPG1_0/D25_1/INT1_1				
131	P000/D16_0/SIN2_1/TIN0_2/PPG0_0/D24_1/INT0_1				
130	C				
129	VSS				
128	VCC5				
127	P134/TRG2/INT5_0/ICU5_0/PPG1_3				
126	P133/SCK1_0/INT3_0/ICU4_0/TOTB1/PPG11_1/TRGS				
125	P132/SOT1_0/INT2_0/ICU3_0/TOTB0				
124	P131/TRG1/SIN1_0/INT4_0/ICU2_0/TIOA1				
123	P130/SCK0_0/INT0_0/ICU1_0/TIOA0				
122	P127/SOT0_0/OCU5_0				
121	P126/TRG0/SIN0_0/INT1_0/OCU4_0				
120	P125/OCU3_0/ICU0_0/PPG10_2				
119	VSS				
118	X1				
117	X0				
116	MD2				
115	MD1				
114	MD0				
113	P124/OCU2_0/ICU5_2/PPG8_2				
112	P085/RX0/INT9_0				
111	P085/TX0/PPG10_1				
110	DEBUGF				
109	VSS				

TOP VIEW
LQFP-144

3. Pin Assignment (LQFP-208)



4. Pin Description (LQFP-144)

Pin Number	Pin Name	I/O Circuit Type	Function Description
2	P015	H/I4 ^{*1}	General-Purpose I/O Port
	D29_0		External Bus Data I/O pin
	SEG5		LCDC Segment(Duty)Output pin
	D21_1		External Bus Data I/O pin
	INT13_1		External Interrupt Request Input pin ch.13 relocation 1
3	P016	H/I4 ^{*1}	General-Purpose I/O Port
	D30_0		External Bus Data I/O pin
	SEG6		LCDC Segment(Duty)Output pin
	D22_1		External Bus Data I/O pin
	INT14_1		External Interrupt Request Input pin ch.14 relocation 1
4	P017	H/I4 ^{*1}	General-Purpose I/O Port
	D31_0		External Bus Data I/O pin
	SEG7		LCDC Segment(Duty)Output pin
	D23_1		External Bus Data I/O pin
	INT15_1		External Interrupt Request Input pin ch.15 relocation 1
5	P020	H/I4 ^{*1}	General-Purpose I/O Port
	ASX		External Bus Address-Strobe Output pin
	SEG8		LCDC Segment(Duty)Output pin
	ICU6_0		Input Capture Input pin ch.6 relocation 0
	OCU0_1		Output Compare Output pin ch.0 relocation 1
6	P021	H/I4 ^{*1}	General-Purpose I/O Port
	CS0X		External Bus Chip-Select 0 Output pin
	SEG9		LCDC Segment(Duty)Output pin
	ICU7_0		Input Capture Input pin ch.7 relocation 0
	OCU1_1		Output Compare Output pin ch.1 relocation 1
7	P022	H/I4 ^{*1}	General-Purpose I/O Port
	CS1X		External Bus Chip-Select 1 Output pin
	SEG10		LCDC Segment(Duty)Output pin
	ICU8_0		Input Capture Input pin ch.8 relocation 0
	OCU2_1		Output Compare Output pin ch.2 relocation 1
8	P023	H/I4 ^{*1}	General-Purpose I/O Port
	RDX		External Bus Read-Strobe Output pin
	SEG11		LCDC Segment(Duty)Output pin
	ICU9_0		Input Capture Input pin ch.9 relocation 0
	OCU3_1		Output Compare Output pin ch.3 relocation 1
9	P024	H/I4 ^{*1}	General-Purpose I/O Port
	WR0X		External Bus Write-Strobe 0 Output pin
	SEG12		LCDC Segment(Duty)Output pin
	ICU10_0		Input Capture Input pin ch.10 relocation 0
	OCU11_0		Output Compare Output pin ch.11 relocation 0

Pin Number	Pin Name	I/O Circuit Type	Function Description
10	P025	H/I4 ¹¹	General-Purpose I/O Port
	WR1X		External Bus Write-Strobe 1 Output pin
	SEG13		LCDC Segment(Duty)Output pin
	ICU11_0		Input Capture Input pin ch.11 relocation 0
	OCU10_0		Output Compare Output pin ch.10 relocation 0
11	P026	H/I4 ¹¹	General-Purpose I/O Port
	A00		External Bus Address Output pin
	SEG14		LCDC Segment(Duty)Output pin
	SPI_CS3		HS_SPI SSEL3 Output pin (Not supported)
	SIN6_1		LIN_UART Serial Input pin ch.6 relocation 1
	OCU9_0		Output Compare Output pin ch.9 relocation 0
12	P027	H/I4 ¹¹	General-Purpose I/O Port
	A01		External Bus Address Output pin
	SEG15		LCDC Segment(Duty)Output pin
	SPI_CS2		HS_SPI SSEL2 Output pin (Not supported)
	SOT6_1		LIN_UART Serial Output pin ch.6 relocation 1
	OCU8_0		Output Compare Output pin ch.8 relocation 0
13	P030	H/I4 ¹¹	General-Purpose I/O Port
	A02		External Bus Address Output pin
	SEG16		LCDC Segment(Duty)Output pin
	SPI_CS1		HS_SPI SSEL1 Output pin (Not supported)
	SCK6_1		LIN_UART Serial Clock I/O pin ch.6 relocation 1
14	P031	H/I4 ¹¹	General-Purpose I/O Port
	A03		External Bus Address Output pin
	SEG17		LCDC Segment(Duty)Output pin
	SPI_CS0		HS_SPI SSEL0 I/O pin (Not supported)
	SIN9_0		Multi-function Serial Input pin ch.9 relocation 0
15	P032	H/I4 ¹¹	General-Purpose I/O Port
	A04		External Bus Address Output pin
	SEG18		LCDC Segment(Duty)Output pin
	SPI_SIO3		HS_SPI SDATA3 I/O pin (Not supported)
	SOT9_0		Multi-function Serial Output pin ch.9 relocation 0
	OCU7_0		Output Compare Output pin ch.7 relocation 0
16	P033	H/I4 ¹¹	General-Purpose I/O Port
	A05		External Bus Address Output pin
	SEG19		LCDC Segment(Duty)Output pin
	SPI_SIO2		HS_SPI SDATA2 I/O pin (Not supported)
	SCK9_0		Multi-function Serial Clock I/O pin ch.9 relocation 0
	OCU6_0		Output Compare Output pin ch.6 relocation 0

Pin Number	Pin Name	I/O Circuit Type	Function Description
17	P034	H/I4 ¹	General-Purpose I/O Port
	A06		External Bus Address Output pin
	SEG20		LCDC Segment(Duty)Output pin
	SPI_SIO1		HS_SPI SDATA1 I/O pin (Not supported)
	SIN8_0		Multi-function Serial Input pin ch.8 relocation 0
	OCU5_1		Output Compare Output pin ch.5 relocation 1
18	P035	H/I4 ¹	General-Purpose I/O Port
	A07		External Bus Address Output pin
	SEG21		LCDC Segment(Duty)Output pin
	SPI_SIO0		HS_SPI SDATA0 I/O pin (Not supported)
	SOT8_0		Multi-function Serial Output pin ch.8 relocation 0
	OCU4_1		Output Compare Output pin ch.4 relocation 1
19	P036	H/I4 ¹	General-Purpose I/O Port
	A08		External Bus Address Output pin
	SEG22		LCDC Segment(Duty)Output pin
	PPG11_0		PPG Output pin ch.11 relocation 0
	SPI_CLK		HS_SPI SCLK I/O pin (Not supported)
	SCK8_0		Multi-function Serial Clock I/O pin ch.8 relocation 0
22	P037	I	General-Purpose I/O Port
	A09		External Bus Address Output pin
	SEG23		LCDC Segment(Duty)Output pin
	ST0		LCDC Segment(Static)Output pin
	PPG12_0		PPG Output pin ch.12 relocation 0
	SIN7_0		LIN_UART Serial Input pin ch.7 relocation 0
23	P040	I	General-Purpose I/O Port
	A10		External Bus Address Output pin
	SEG24		LCDC Segment(Duty)Output pin
	ST1		LCDC Segment(Static)Output pin
	PPG13_0		PPG Output pin ch.13 relocation 0
	SOT7_0		LIN_UART Serial Output pin ch.7 relocation 0
24	P041	I	General-Purpose I/O Port
	A11		External Bus Address Output pin
	SEG25		LCDC Segment(Duty)Output pin
	ST2		LCDC Segment(Static)Output pin
	PPG14_0		PPG Output pin ch.14 relocation 0
	SCK7_0		LIN_UART Serial Clock I/O pin ch.7 relocation 0
25	P042	I	General-Purpose I/O Port
	A12		External Bus Address Output pin
	SEG26		LCDC Segment(Duty)Output pin
	ST3		LCDC Segment(Static)Output pin
	PPG15_0		PPG Output pin ch.15 relocation 0
	AIN0_0		Up/down Counter AIN Input pin ch.0 relocation 0

Pin Number	Pin Name	I/O Circuit Type	Function Description
26	P043	I	General-Purpose I/O Port
	A13		External Bus Address Output pin
	SEG27		LCDC Segment(Duty)Output pin
	ST4		LCDC Segment(Static)Output pin
	BIN0_0		Up/down Counter BIN Input pin ch.0 relocation 0
	SGA4_0		Sound Generator SGA Output pin ch.4 relocation 0
	OCU6_1		Output Compare Output pin ch.6 relocation 1
27	P044	I	General-Purpose I/O Port
	A14		External Bus Address Output pin
	SEG28		LCDC Segment(Duty)Output pin
	ST5		LCDC Segment(Static)Output pin
	ZIN0_0		Up/down Counter ZIN Input pin ch.0 relocation 0
	SGO4_0		Sound Generator SGO Output pin ch.4 relocation 0
	OCU7_1		Output Compare Output pin ch.7 relocation 1
28	P045	I	General-Purpose I/O Port
	A15		External Bus Address Output pin
	SEG29		LCDC Segment(Duty)Output pin
	ST6		LCDC Segment(Static)Output pin
	AIN1_0		Up/down Counter AIN Input pin ch.1 relocation 0
	SIN8_2		Multi-function Serial Input pin ch.8 relocation 2
29	P046	I	General-Purpose I/O Port
	A16		External Bus Address Output pin
	SEG30		LCDC Segment(Duty)Output pin
	ST7		LCDC Segment(Static)Output pin
	BIN1_0		Up/down Counter BIN Input pin ch.1 relocation 0
	SOT8_2		Multi-function Serial Output pin ch.8 relocation 2
30	P047	I	General-Purpose I/O Port
	A17		External Bus Address Output pin
	SEG31		LCDC Segment(Duty)Output pin
	ST8		LCDC Segment(Static)Output pin
	ZIN1_0		Up/down Counter ZIN Input pin ch.1 relocation 0
	SCK8_2		Multi-function Serial Clock I/O pin ch.8 relocation 2
31	P050	I	General-Purpose I/O Port
	A18		External Bus Address Output pin
	COM0		LCDC Segment(Duty)Common Output pin
	OCU8_1		Output Compare Output pin ch.8 relocation 1
32	P051	I	General-Purpose I/O Port
	A19		External Bus Address Output pin
	COM1		LCDC Segment(Duty)Common Output pin
	OCU9_1		Output Compare Output pin ch.9 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
33	P052	I	General-Purpose I/O Port
	A20		External Bus Address Output pin
	COM2		LCDC Segment(Duty)Common Output pin
	OCU10_1		Output Compare Output pin ch.10 relocation 1
34	P053	I	General-Purpose I/O Port
	A21		External Bus Address Output pin
	COM3		LCDC Segment(Duty)Common Output pin
	OCU11_1		Output Compare Output pin ch.11 relocation 1
35	P054	I2	General-Purpose I/O Port
	SYSCLK		External Bus Clock Output pin
	V0		LCDC Reference Voltage V0 Input pin
	FRCK0_1		Free-Run Timer Clock Input pin ch.0 relocation 1
38	P055	I2	General-Purpose I/O Port
	CS2X		External Bus Chip-Select 2 Output pin
	V1		LCDC Reference Voltage V1 Input pin
	FRCK1_1		Free-Run Timer Clock Input pin ch.1 relocation 1
39	P056	I2	General-Purpose I/O Port
	CS3X		External Bus Chip-Select 3 Output pin
	V2		LCDC Reference Voltage V2 Input pin
	FRCK2_1		Free-Run Timer Clock Input pin ch.2 relocation 1
40	P057	I3	General-Purpose I/O Port (Input only. No output.)
	RDY		External Bus RDY Input pin
	V3		LCDC Reference Voltage V3 Input pin
	FRCK3_1		Free-Run Timer Clock Input pin ch.3 relocation 1
43	P060	K	General-Purpose I/O Port
	PWM1P0		SMC Output pin ch.0
	AN8		ADC Analog Input pin ch.8
44	P061	K	General-Purpose I/O Port
	PWM1M0		SMC Output pin ch.0
	AN9		ADC Analog Input pin ch.9
	SIN1_1		Multi-function Serial Input pin ch.1 relocation 1
45	P062	K	General-Purpose I/O Port
	PWM2P0		SMC Output pin ch.0
	AN10		ADC Analog Input pin ch.10
	ZIN1_1		Up/down Counter ZIN Input pin ch.1 relocation 1
	SOT1_1		Multi-function Serial Output pin ch.1 relocation 1
46	P063	K	General-Purpose I/O Port
	PWM2M0		SMC Output pin ch.0
	AN11		ADC Analog Input pin ch.11
	BIN1_1		Up/down Counter BIN Input pin ch.1 relocation 1
	SCK1_1		Multi-function Serial Clock I/O pin ch.1 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
47	P064	K	General-Purpose I/O Port
	PWM1P1		SMC Output pin ch.1
	AN12		ADC Analog Input pin ch.12
	AIN1_1		Up/down Counter AIN Input pin ch.1 relocation 1
	SIN0_1		Multi-function Serial Input pin ch.0 relocation 1
48	P065	K	General-Purpose I/O Port
	PWM1M1		SMC Output pin ch.1
	AN13		ADC Analog Input pin ch.13
	ZIN0_1		Up/down Counter ZIN Input pin ch.0 relocation 1
	SOT0_1		Multi-function Serial Output pin ch.0 relocation 1
49	P066	K	General-Purpose I/O Port
	PWM2P1		SMC Output pin ch.1
	AN14		ADC Analog Input pin ch.14
	BIN0_1		Up/down Counter BIN Input pin ch.0 relocation 1
	SCK0_1		Multi-function Serial Clock I/O pin ch.0 relocation 1
50	P067	K	General-Purpose I/O Port
	PWM2M1		SMC Output pin ch.1
	AN15		ADC Analog Input pin ch.15
	AIN0_1		Up/down Counter AIN Input pin ch.0 relocation 1
	SIN9_1		Multi-function Serial Input pin ch.9 relocation 1
53	P070	K	General-Purpose I/O Port
	PWM1P2		SMC Output pin ch.2
	AN16		ADC Analog Input pin ch.16
	SOT9_1		Multi-function Serial Output pin ch.9 relocation 1
54	P071	K	General-Purpose I/O Port
	PWM1M2		SMC Output pin ch.2
	AN17		ADC Analog Input pin ch.17
	SCK9_1		Multi-function Serial Clock I/O pin ch.9 relocation 1
55	P072	K	General-Purpose I/O Port
	PWM2P2		SMC Output pin ch.2
	AN18		ADC Analog Input pin ch.18
	ICU11_1		Input Capture Input pin ch.11 relocation 1
	SIN8_1		Multi-function Serial Input pin ch.8 relocation 1
56	P073	K	General-Purpose I/O Port
	PWM2M2		SMC Output pin ch.2
	AN19		ADC Analog Input pin ch.19
	ICU10_1		Input Capture Input pin ch.10 relocation 1
	SOT8_1		Multi-function Serial Output pin ch.8 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
57	P074	K	General-Purpose I/O Port
	PWM1P3		SMC Output pin ch.3
	AN20		ADC Analog Input pin ch.20
	PPG12_1		PPG Output pin ch.12 relocation 1
	ICU9_1		Input Capture Input pin ch.9 relocation 1
	SCK8_1		Multi-function Serial Clock I/O pin ch.8 relocation 1
58	P075	K	General-Purpose I/O Port
	PWM1M3		SMC Output pin ch.3
	AN21		ADC Analog Input pin ch.21
	PPG13_1		PPG Output pin ch.13 relocation 1
	ICU8_1		Input Capture Input pin ch.8 relocation 1
	SIN7_1		LIN_UART Serial Input pin ch.7 relocation 1
59	P076	K	General-Purpose I/O Port
	PWM2P3		SMC Output pin ch.3
	AN22		ADC Analog Input pin ch.22
	PPG14_1		PPG Output pin ch.14 relocation 1
	ICU7_1		Input Capture Input pin ch.7 relocation 1
	SOT7_1		LIN_UART Serial Output pin ch.7 relocation 1
60	P077	K	General-Purpose I/O Port
	PWM2M3		SMC Output pin ch.3
	AN23		ADC Analog Input pin ch.23
	PPG15_1		PPG Output pin ch.15 relocation 1
	ICU6_1		Input Capture Input pin ch.6 relocation 1
	SCK7_1		LIN_UART Serial Clock I/O pin ch.7 relocation 1
63	P080	K	General-Purpose I/O Port
	PWM1P4		SMC Output pin ch.4
	AN24		ADC Analog Input pin ch.24
	SIN6_0		LIN_UART Serial Input pin ch.6 relocation 0
	PPG16_0		PPG Output pin ch.16 relocation 0
	AIN0_2		Up/down Counter AIN Input pin ch.0 relocation 2
64	P081	K	General-Purpose I/O Port
	PWM1M4		SMC Output pin ch.4
	AN25		ADC Analog Input pin ch.25
	SOT6_0		LIN_UART Serial Output pin ch.6 relocation 0
	PPG17_0		PPG Output pin ch.17 relocation 0
	BIN0_2		Up/down Counter BIN Input pin ch.0 relocation 2
65	P082	K	General-Purpose I/O Port
	PWM2P4		SMC Output pin ch.4
	AN26		ADC Analog Input pin ch.26
	SCK6_0		LIN_UART Serial Clock I/O pin ch.6 relocation 0
	PPG18_0		PPG Output pin ch.18 relocation 0
	ZIN0_2		Up/down Counter ZIN Input pin ch.0 relocation 2

Pin Number	Pin Name	I/O Circuit Type	Function Description
66	P083	K	General-Purpose I/O Port
	PWM2M4		SMC Output pin ch.4
	AN27		ADC Analog Input pin ch.27
	ICU0_2		Input Capture Input pin ch.0 relocation 2
	PPG19_0		PPG Output pin ch.19 relocation 0
67	P084	K	General-Purpose I/O Port
	PWM1P5		SMC Output pin ch.5
	AN28		ADC Analog Input pin ch.28
	ICU1_2		Input Capture Input pin ch.1 relocation 2
	PPG20_0		PPG Output pin ch.20 relocation 0
68	P085	K	General-Purpose I/O Port
	PWM1M5		SMC Output pin ch.5
	AN29		ADC Analog Input pin ch.29
	ICU2_2		Input Capture Input pin ch.2 relocation 2
	PPG21_0		PPG Output pin ch.21 relocation 0
69	P086	K	General-Purpose I/O Port
	PWM2P5		SMC Output pin ch.5
	AN30		ADC Analog Input pin ch.30
	ICU3_2		Input Capture Input pin ch.3 relocation 2
	PPG22_0		PPG Output pin ch.22 relocation 0
70	P087	K	General-Purpose I/O Port
	PWM2M5		SMC Output pin ch.5
	AN31		ADC Analog Input pin ch.31
	ICU4_2		Input Capture Input pin ch.4 relocation 2
	PPG23_0		PPG Output pin ch.23 relocation 0
73	P090	M	General-Purpose I/O Port
	ADTG		ADC External Trigger Input pin
	PPG0_2		PPG Output pin ch.0 relocation 2
74	P100	J	General-Purpose I/O Port
	SIN4_1		LIN_UART Serial Input pin ch.4 relocation 1
	AN0		ADC Analog Input pin ch.0
	TIN0_1		Reload Timer Event Input pin ch.0 relocation 1
	PPG8_0		PPG Output pin ch.8 relocation 0
75	P101	J	General-Purpose I/O Port
	SOT4_1		LIN_UART Serial Output pin ch.4 relocation 1
	AN1		ADC Analog Input pin ch.1
	TIN1_1		Reload Timer Event Input pin ch.1 relocation 1
	PPG9_0		PPG Output pin ch.9 relocation 0

Pin Number	Pin Name	I/O Circuit Type	Function Description
76	P102	J	General-Purpose I/O Port
	SCK4_1		LIN_UART Serial Clock I/O pin ch.4 relocation 1
	AN2		ADC Analog Input pin ch.2
	TIN2_1		Reload Timer Event Input pin ch.2 relocation 1
	PPG10_0		PPG Output pin ch.10 relocation 0
	ICU6_2		Input Capture Input pin ch.6 relocation 2
77	P103	J	General-Purpose I/O Port
	SIN5_1		LIN_UART Serial Input pin ch.5 relocation 1
	AN3		ADC Analog Input pin ch.3
	TIN3_1		Reload Timer Event Input pin ch.3 relocation 1
	PPG1_1		PPG Output pin ch.1 relocation 1
	ICU7_2		Input Capture Input pin ch.7 relocation 2
78	P104	J	General-Purpose I/O Port
	SOT5_1		LIN_UART Serial Output pin ch.5 relocation 1
	AN4		ADC Analog Input pin ch.4
	TOT0_1		Reload Timer Output pin ch.0 relocation 1
	PPG2_1		PPG Output pin ch.2 relocation 1
	ICU8_2		Input Capture Input pin ch.8 relocation 2
79	P105	J	General-Purpose I/O Port
	SCK5_1		LIN_UART Serial Clock I/O pin ch.5 relocation 1
	AN5		ADC Analog Input pin ch.5
	TOT1_1		Reload Timer Output pin ch.1 relocation 1
	PPG3_1		PPG Output pin ch.3 relocation 1
	ICU9_2		Input Capture Input pin ch.9 relocation 2
80	P106	J	General-Purpose I/O Port
	AN6		ADC Analog Input pin ch.6
	PPG4_1		PPG Output pin ch.4 relocation 1
	ICU10_2		Input Capture Input pin ch.10 relocation 2
	SGA4_1		Sound Generator SGA Output pin ch.4 relocation 1
81	P107	L	General-Purpose I/O Port
	AN7		ADC Analog Input pin ch.7
	PPG5_1		PPG Output pin ch.5 relocation 1
	DAO1		DAC Output pin ch.1
	ICU11_2		Input Capture Input pin ch.11 relocation 2
	SGO4_1		Sound Generator SGO Output pin ch.4 relocation 1
85	P123	L	General-Purpose I/O Port
	OCU1_0		Output Compare Output pin ch.1 relocation 0
	PPG8_2		PPG Output pin ch.8 relocation 2
	DAO0		DAC Output pin ch.0
	AN39		ADC Analog Input pin ch.39

Pin Number	Pin Name	I/O Circuit Type	Function Description
86	P122	J	General-Purpose I/O Port
	OCU0_0		Output Compare Output pin ch.0 relocation 0
	SCK5_0		LIN_UART Serial Clock I/O pin ch.5 relocation 0
	TOT3_0		Reload Timer Output pin ch.3 relocation 0
	PPG7_2		PPG Output pin ch.7 relocation 2
	AN38		ADC Analog Input pin ch.38
87	P121	J	General-Purpose I/O Port
	FRCK0_0		Free-Run Timer Clock Input pin ch.0 relocation 0
	SOT5_0		LIN_UART Serial Output pin ch.5 relocation 0
	INT7_0		External Interrupt Request Input pin ch.7 relocation 0
	TOT2_0		Reload Timer Output pin ch.2 relocation 0
	PPG6_2		PPG Output pin ch.6 relocation 2
	AN37		ADC Analog Input pin ch.37
88	P120	J	General-Purpose I/O Port
	FRCK1_0		Free-Run Timer Clock Input pin ch.1 relocation 0
	SIN5_0		LIN_UART Serial Input pin ch.5 relocation 0
	INT6_0		External Interrupt Request Input pin ch.6 relocation 0
	TOT1_0		Reload Timer Output pin ch.1 relocation 0
	PPG5_2		PPG Output pin ch.5 relocation 2
	AN36		ADC Analog Input pin ch.36
89	P117	J	General-Purpose I/O Port
	SCK4_0		LIN_UART Serial Clock I/O pin ch.4 relocation 0
	TOT0_0		Reload Timer Output pin ch.0 relocation 0
	SGO3		Sound Generator SGO Output pin ch.3
	TRG4		PPG Trigger Input pin 4 (ch.16-ch.19)
	FRCK2_0		Free-Run Timer Clock Input pin ch.2 relocation 0
	AN35		ADC Analog Input pin ch.35
90	P116	J	General-Purpose I/O Port
	SOT4_0		LIN_UART Serial Output pin ch.4 relocation 0
	TIN3_0		Reload Timer Event Input pin ch.3 relocation 0
	SGA3		Sound Generator SGA Output pin ch.3
	FRCK3_0		Free-Run Timer Clock Input pin ch.3 relocation 0
	AN34		ADC Analog Input pin ch.34
91	P115	J	General-Purpose I/O Port
	SIN4_0		LIN_UART Serial Input pin ch.4 relocation 0
	TIN2_0		Reload Timer Event Input pin ch.2 relocation 0
	SGO2		Sound Generator SGO Output pin ch.2
	FRCK4_0		Free-Run Timer Clock Input pin ch.4 relocation 0
	AN33		ADC Analog Input pin ch.33

Pin Number	Pin Name	I/O Circuit Type	Function Description
92	P114	J	General-Purpose I/O Port
	SCK3_0		LIN_UART Serial Clock I/O pin ch.3 relocation 0
	TIN1_0		Reload Timer Event Input pin ch.1 relocation 0
	ICU5_1		Input Capture Input pin ch.5 relocation 1
	SGA2		Sound Generator SGA Output pin ch.2
	TRG3		PPG Trigger Input pin 3 (ch.12-ch.15)
	AN32		ADC Analog Input pin ch.32
95	P137	M (Y)	General-Purpose I/O Port
	(X0A)		Sub Clock oscillation Input pin (only dual clock product)
96	P136	M (Y)	General-Purpose I/O Port
	(X1A)		Sub Clock oscillation Output pin (only dual clock product)
97	NMIX	R	NMI Pin
98	P097	M	General-Purpose I/O Port
	WOT		RTC Overflow Output pin
	SOT3_0		LIN_UART Serial Output pin ch.3 relocation 0
	INT8_0		External Interrupt Request Input pin ch.8 relocation 0
	TIN0_0		Reload Timer Event Input pin ch.0 relocation 0
	ICU4_1		Input Capture Input pin ch.4 relocation 1
	PPG0_1		PPG Output pin ch.0 relocation 1
99	P094	M	General-Purpose I/O Port
	SGO1		Sound Generator SGO Output pin ch.1
	SIN3_0		LIN_UART Serial Input pin ch.3 relocation 0
	INT15_0		External Interrupt Request Input pin ch.15 relocation 0
	ICU1_1		Input Capture Input pin ch.1 relocation 1
	PPG9_1		PPG Output pin ch.9 relocation 1
100	P093	M	General-Purpose I/O Port
	SGA1		Sound Generator SGA Output pin ch.1
	SOT2_0		LIN_UART Serial Output pin ch.2 relocation 0
	INT14_0		External Interrupt Request Input pin ch.14 relocation 0
	ICU3_1		Input Capture Input pin ch.3 relocation 1
	PPG8_1		PPG Output pin ch.8 relocation 1
101	P092	M	General-Purpose I/O Port
	SGO0		Sound Generator SGO Output pin ch.0
	SCK2_0		LIN_UART Serial Clock I/O pin ch.2 relocation 0
	INT13_0		External Interrupt Request Input pin ch.13 relocation 0
	TOT3_1		Reload Timer Output pin ch.3 relocation 1
	ICU0_1		Input Capture Input pin ch.0 relocation 1
	PPG7_1		PPG Output pin ch.7 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
102	P091	M	General-Purpose I/O Port
	SGA0		Sound Generator SGA Output pin ch.0
	SIN2_0		LIN_UART Serial Input pin ch.2 relocation 0
	INT12_0		External Interrupt Request Input pin ch.12 relocation 0
	TOT2_1		Reload Timer Output pin ch.2 relocation 1
	ICU2_1		Input Capture Input pin ch.2 relocation 1
	PPG6_1		PPG Output pin ch.6 relocation 1
103	P110	M	General-Purpose I/O Port
	TX1		CAN TX Data Output pin ch.1
	PPG1_2		PPG Output pin ch.1 relocation 2
	FRCK5_0		Free-Run Timer Clock Input pin ch.5 relocation 0
104	P111	M	General-Purpose I/O Port
	RX1		CAN RX Data Input pin ch.1
	INT10_0		External Interrupt Request Input pin ch.10 relocation 0
	PPG2_2		PPG Output pin ch.2 relocation 2
105	P112	M	General-Purpose I/O Port
	TX2		CAN TX Data Output pin ch.2
	PPG3_2		PPG Output pin ch.3 relocation 2
106	P113	M	General-Purpose I/O Port
	RX2		CAN RX Data Input pin ch.2
	INT11_0		External Interrupt Request Input pin ch.11 relocation 0
	PPG4_2		PPG Output pin ch.4 relocation 2
107	RSTX	R	Reset Pin
110	DEBUGIF	B	DEBUG I/F pin
111	P095	M	General-Purpose I/O Port
	TX0		CAN TX Data Output pin ch.0
	PPG10_1		PPG Output pin ch.10 relocation 1
112	P096	M	General-Purpose I/O Port
	RX0		CAN RX Data Input pin ch.0
	INT9_0		External Interrupt Request Input pin ch.9 relocation 0
113	P124	M	General-Purpose I/O Port
	OCU2_0		Output Compare Output pin ch.2 relocation 0
	ICU5_2		Input Capture Input pin ch.5 relocation 2
	PPG9_2		PPG Output pin ch.9 relocation 2
114	MD0	A	Mode Pin 0
115	MD1	A	Mode Pin 1
116	MD2	R2	Mode Pin 2
117	X0	X	Main Clock oscillation Input pin
118	X1	X	Main Clock oscillation Output pin
120	P125	M	General-Purpose I/O Port
	OCU3_0		Output Compare Output pin ch.3 relocation 0
	ICU0_0		Input Capture Input pin ch.0 relocation 0
	PPG10_2		PPG Output pin ch.10 relocation 2

Pin Number	Pin Name	I/O Circuit Type	Function Description
121	P126	M	General-Purpose I/O Port
	TRG0		PPG Trigger Input pin 0 (ch.0-ch.3)
	SIN0_0		Multi-function Serial Input pin ch.0 relocation 0
	INT1_0		External Interrupt Request Input pin ch.1 relocation 0
	OCU4_0		Output Compare Output pin ch.4 relocation 0
122	P127	N	General-Purpose I/O Port
	SOT0_0		Multi-function Serial Output pin ch.0 relocation 0
	OCU5_0		Output Compare Output pin ch.5 relocation 0
123	P130	N	General-Purpose I/O Port
	SCK0_0		Multi-function Serial Clock I/O pin ch.0 relocation 0
	INT0_0		External Interrupt Request Input pin ch.0 relocation 0
	ICU1_0		Input Capture Input pin ch.1 relocation 0
	TIOA0		Base Timer Output pin ch.0
124	P131	M	General-Purpose I/O Port
	TRG1		PPG Trigger Input pin 1 (ch.4-ch.7)
	SIN1_0		Multi-function Serial Input pin ch.1 relocation 0
	INT4_0		External Interrupt Request Input pin ch.4 relocation 0
	ICU2_0		Input Capture Input pin ch.2 relocation 0
	TIOA1		Base Timer I/O pin ch.1
125	P132	N	General-Purpose I/O Port
	SOT1_0		Multi-function Serial Output pin ch.1 relocation 0
	INT2_0		External Interrupt Request Input pin ch.2 relocation 0
	ICU3_0		Input Capture Input pin ch.3 relocation 0
	TIOB0		Base Timer Input pin ch.0
126	P133	N	General-Purpose I/O Port
	SCK1_0		Multi-function Serial Clock I/O pin ch.1 relocation 0
	INT3_0		External Interrupt Request Input pin ch.3 relocation 0
	ICU4_0		Input Capture Input pin ch.4 relocation 0
	TIOB1		Base Timer Input pin ch.1
	PPG11_1		PPG Output pin ch.11 relocation 1
	TRG5		PPG Trigger Input pin 5 (ch.20-ch.23)
127	P134	M	General-Purpose I/O Port
	TRG2		PPG Trigger Input pin 2 (ch.8-ch.11)
	INT5_0		External Interrupt Request Input pin ch.5 relocation 0
	ICU5_0		Input Capture Input pin ch.5 relocation 0
	PPG1_3		PPG Output pin ch.1 relocation 3
131	P000	M	General-Purpose I/O Port
	D16_0		External Bus Data I/O pin
	SIN2_1		LIN_UART Serial Input pin ch.2 relocation 1
	TIN0_2		Reload Timer Event Input pin ch.0 relocation 2
	PPG0_0		PPG Output pin ch.0 relocation 0
	D24_1		External Bus Data I/O pin
	INT0_1		External Interrupt Request Input pin ch.0 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
132	P001	M	General-Purpose I/O Port
	D17_0		External Bus Data I/O pin
	SOT2_1		LIN_UART Serial Output pin ch.2 relocation 1
	TIN1_2		Reload Timer Event Input pin ch.1 relocation 2
	PPG1_0		PPG Output pin ch.1 relocation 0
	D25_1		External Bus Data I/O pin
	INT1_1		External Interrupt Request Input pin ch.1 relocation 1
133	P002	M	General-Purpose I/O Port
	D18_0		External Bus Data I/O pin
	SCK2_1		LIN_UART Serial Clock I/O pin ch.2 relocation 1
	TIN2_2		Reload Timer Event Input pin ch.2 relocation 2
	PPG2_0		PPG Output pin ch.2 relocation 0
	D26_1		External Bus Data I/O pin
	INT2_1		External Interrupt Request Input pin ch.2 relocation 1
134	P003	M	General-Purpose I/O Port
	D19_0		External Bus Data I/O pin
	SIN3_1		LIN_UART Serial Input pin ch.3 relocation 1
	TIN3_2		Reload Timer Event Input pin ch.3 relocation 2
	PPG3_0		PPG Output pin ch.3 relocation 0
	D27_1		External Bus Data I/O pin
	INT3_1		External Interrupt Request Input pin ch.3 relocation 1
135	P004	M	General-Purpose I/O Port
	D20_0		External Bus Data I/O pin
	SOT3_1		LIN_UART Serial Output pin ch.3 relocation 1
	TOT0_2		Reload Timer Output pin ch.0 relocation 2
	PPG4_0		PPG Output pin ch.4 relocation 0
	D28_1		External Bus Data I/O pin
	INT4_1		External Interrupt Request Input pin ch.4 relocation 1
136	P005	M	General-Purpose I/O Port
	D21_0		External Bus Data I/O pin
	SCK3_1		LIN_UART Serial Clock I/O pin ch.3 relocation 1
	TOT1_2		Reload Timer Output pin ch.1 relocation 2
	PPG5_0		PPG Output pin ch.5 relocation 0
	D29_1		External Bus Data I/O pin
	INT5_1		External Interrupt Request Input pin ch.5 relocation 1
137	P006	M	General-Purpose I/O Port
	D22_0		External Bus Data I/O pin
	TOT2_2		Reload Timer Output pin ch.2 relocation 2
	PPG6_0		PPG Output pin ch.6 relocation 0
	D30_1		External Bus Data I/O pin
	INT6_1		External Interrupt Request Input pin ch.6 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
138	P007	M	General-Purpose I/O Port
	D23_0		External Bus Data I/O pin
	TOT3_2		Reload Timer Output pin ch.3 relocation 2
	PPG7_0		PPG Output pin ch.7 relocation 0
	D31_1		External Bus Data I/O pin
	INT7_1		External Interrupt Request Input pin ch.7 relocation 1
139	P010	H/I4 ¹	General-Purpose I/O Port
	D24_0		External Bus Data I/O pin
	SEG0		LCDC Segment(Duty)Output pin
	D16_1		External Bus Data I/O pin
	INT8_1		External Interrupt Request Input pin ch.8 relocation 1
140	P011	H/I4 ¹	General-Purpose I/O Port
	D25_0		External Bus Data I/O pin
	SEG1		LCDC Segment(Duty)Output pin
	D17_1		External Bus Data I/O pin
	INT9_1		External Interrupt Request Input pin ch.9 relocation 1
141	P012	H/I4 ¹	General-Purpose I/O Port
	D26_0		External Bus Data I/O pin
	SEG2		LCDC Segment(Duty)Output pin
	D18_1		External Bus Data I/O pin
	INT10_1		External Interrupt Request Input pin ch.10 relocation 1
142	P013	H/I4 ¹	General-Purpose I/O Port
	D27_0		External Bus Data I/O pin
	SEG3		LCDC Segment(Duty)Output pin
	D19_1		External Bus Data I/O pin
	INT11_1		External Interrupt Request Input pin ch.11 relocation 1
143	P014	H/I4 ¹	General-Purpose I/O Port
	D28_0		External Bus Data I/O pin
	SEG4		LCDC Segment(Duty)Output pin
	D20_1		External Bus Data I/O pin
	INT12_1		External Interrupt Request Input pin ch.12 relocation 1
1	VCCE	-	+3.3v/+5.0v Power Supply pin
20	VCCE	-	+3.3v/+5.0v Power Supply pin
21	VSS	-	GND pin
36	VCC5	-	+5.0v Power Supply pin
37	VSS	-	GND pin
41	DVCC	-	Power Supply pin for SMC high current
42	DVSS	-	GND pin for SMC high current
51	DVCC	-	Power Supply pin for SMC high current
52	DVSS	-	GND pin for SMC high current
61	DVCC	-	Power Supply pin for SMC high current
62	DVSS	-	GND pin for SMC high current
71	DVCC	-	Power Supply pin for SMC high current

Pin Number	Pin Name	I/O Circuit Type	Function Description
72	DVSS	-	GND pin for SMC high current
82	AVSS/AVRL	-	ADC, DAC GND pin / Low Reference Voltage pin
83	AVRH	-	ADC High Reference Voltage pin
84	AVCC	-	ADC, DAC Analog Power Supply pin
93	VCC5	-	+5.0v Power Supply pin
94	VSS	-	GND pin
108	VCC5	-	+5.0v Power Supply pin
109	VSS	-	GND pin
119	VSS	-	GND pin
128	VCC5	-	+5.0v Power Supply pin
129	VSS	-	GND pin
130	C	-	External Capacitance Connection Pin
144	VSS	-	GND pin

*1: I/O circuit type H is applied to CY91F575/7 and type I4 applied to CY91F578/9.

5. Pin Description (LQFP-208)

Pin Number	Pin Name	I/O Circuit Type	Function Description
1	VCCE	-	+3.3v/+5.0v Power Supply pin
2	P171	M2	General-Purpose I/O Port
	A03		External Bus Address Output pin
3	P172	M2	General-Purpose I/O Port
	A04		External Bus Address Output pin
4	P173	M2	General-Purpose I/O Port
	A05		External Bus Address Output pin
5	P174	M2	General-Purpose I/O Port
	A06		External Bus Address Output pin
6	P175	M2	General-Purpose I/O Port
	A07		External Bus Address Output pin
7	P176	M2	General-Purpose I/O Port
	A08		External Bus Address Output pin
8	P177	M2	General-Purpose I/O Port
	A09		External Bus Address Output pin
9	P180	M2	General-Purpose I/O Port
	A10		External Bus Address Output pin
10	P181	M2	General-Purpose I/O Port
	A11		External Bus Address Output pin
11	P182	M2	General-Purpose I/O Port
	A12		External Bus Address Output pin
12	P183	M2	General-Purpose I/O Port
	A13		External Bus Address Output pin
13	P184	M2	General-Purpose I/O Port
	A14		External Bus Address Output pin
14	P185	M2	General-Purpose I/O Port
	A15		External Bus Address Output pin
15	P186	M2	General-Purpose I/O Port
	A16		External Bus Address Output pin
16	P187	M2	General-Purpose I/O Port
	A17		External Bus Address Output pin
17	P190	M2	General-Purpose I/O Port
	A18		External Bus Address Output pin
18	P191	M2	General-Purpose I/O Port
	A19		External Bus Address Output pin
19	P192	M2	General-Purpose I/O Port
	A20		External Bus Address Output pin
20	P193	M2	General-Purpose I/O Port
	A21		External Bus Address Output pin
21	VCCE	-	+3.3v/+5.0v Power Supply pin
22	VSS	-	GND pin
23	P194	M2	General-Purpose I/O Port
	SYCLK		External Bus Clock Output pin
24	P195	M2	General-Purpose I/O Port
	CS2X		External Bus Chip-Select 2 Output pin
25	P196	M2	General-Purpose I/O Port
	CS3X		External Bus Chip-Select 3 Output pin
26	P197	M2	General-Purpose I/O Port
	RDY		External Bus RDY Input pin

Pin Number	Pin Name	I/O Circuit Type	Function Description
27	VCC5	-	+5.0v Power Supply pin
28	VSS	-	GND pin
29	P010	H	General-Purpose I/O Port
	SEG0		LCDC Segment(Duty)Output pin
29	INT8_1	H	External Interrupt Request Input pin ch.8 relocation 1
30	P011	I	General-Purpose I/O Port
	SEG1		LCDC Segment(Duty)Output pin
	INT9_1		External Interrupt Request Input pin ch.9 relocation 1
31	P012	I	General-Purpose I/O Port
	SEG2		LCDC Segment(Duty)Output pin
	INT10_1		External Interrupt Request Input pin ch.10 relocation 1
32	P013	I	General-Purpose I/O Port
	SEG3		LCDC Segment(Duty)Output pin
	INT11_1		External Interrupt Request Input pin ch.11 relocation 1
33	P014	I	General-Purpose I/O Port
	SEG4		LCDC Segment(Duty)Output pin
	INT12_1		External Interrupt Request Input pin ch.12 relocation 1
34	P015	I	General-Purpose I/O Port
	SEG5		LCDC Segment(Duty)Output pin
	INT13_1		External Interrupt Request Input pin ch.13 relocation 1
35	P016	I	General-Purpose I/O Port
	SEG6		LCDC Segment(Duty)Output pin
	INT14_1		External Interrupt Request Input pin ch.14 relocation 1
36	P017	I	General-Purpose I/O Port
	SEG7		LCDC Segment(Duty)Output pin
	INT15_1		External Interrupt Request Input pin ch.15 relocation 1
37	P020	I	General-Purpose I/O Port
	SEG8		LCDC Segment(Duty)Output pin
	ICU6_0		Input Capture Input pin ch.6 relocation 0
	OCU0_1		Output Compare Output pin ch.0 relocation 1
38	P021	I	General-Purpose I/O Port
	SEG9		LCDC Segment(Duty)Output pin
	ICU7_0		Input Capture Input pin ch.7 relocation 0
	OCU1_1		Output Compare Output pin ch.1 relocation 1
39	P022	I	General-Purpose I/O Port
	SEG10		LCDC Segment(Duty)Output pin
	ICU8_0		Input Capture Input pin ch.8 relocation 0
	OCU2_1		Output Compare Output pin ch.2 relocation 1
40	P023	I	General-Purpose I/O Port
	SEG11		LCDC Segment(Duty)Output pin
	ICU9_0		Input Capture Input pin ch.9 relocation 0
	OCU3_1		Output Compare Output pin ch.3 relocation 1
41	P024	I	General-Purpose I/O Port
	SEG12		LCDC Segment(Duty)Output pin
	ICU10_0		Input Capture Input pin ch.10 relocation 0
	OCU11_0		Output Compare Output pin ch.11 relocation 0
42	P025	I	General-Purpose I/O Port
	SEG13		LCDC Segment(Duty)Output pin
	ICU11_0		Input Capture Input pin ch.11 relocation 0
	OCU10_0		Output Compare Output pin ch.10 relocation 0

Pin Number	Pin Name	I/O Circuit Type	Function Description
43	P026	I	General-Purpose I/O Port
	SEG14		LCDC Segment(Duty)Output pin
	SIN6_1		LIN_UART Serial Input pin ch.6 relocation 1
	OCU9_0		Output Compare Output pin ch.9 relocation 0
44	P027	I	General-Purpose I/O Port
	SEG15		LCDC Segment(Duty)Output pin
	SOT6_1		LIN_UART Serial Output pin ch.6 relocation 1
	OCU8_0		Output Compare Output pin ch.8 relocation 8
45	P030	I	General-Purpose I/O Port
45	SEG16	I	LCDC Segment(Duty)Output pin
	SCK6_1		LIN_UART Serial Clock I/O pin ch.6 relocation 1
46	P031	I	General-Purpose I/O Port
	SEG17		LCDC Segment(Duty)Output pin
	SIN9_0		Multi-function Serial Input pin ch.9 relocation 0
47	P032	I	General-Purpose I/O Port
	SEG18		LCDC Segment(Duty)Output pin
	SOT9_0		Multi-function Serial Output pin ch.9 relocation 0
	OCU7_0		Output Compare Output pin ch.7 relocation 7
48	P033	I	General-Purpose I/O Port
	SEG19		LCDC Segment(Duty)Output pin
	SCK9_0		Multi-function Serial Clock I/O pin ch.9 relocation 0
	OCU6_0		Output Compare Output pin ch.6 relocation 6
49	P034	I	General-Purpose I/O Port
	SEG20		LCDC Segment(Duty)Output pin
	SIN8_0		Multi-function Serial Input pin ch.8 relocation 0
	OCU5_1		Output Compare Output pin ch.5 relocation 1
50	P035	I	General-Purpose I/O Port
	SEG21		LCDC Segment(Duty)Output pin
	SOT8_0		Multi-function Serial Output pin ch.8 relocation 0
	OCU4_1		Output Compare Output pin ch.4 relocation 1
51	P036	I	General-Purpose I/O Port
	SEG22		LCDC Segment(Duty)Output pin
	PPG11_0		PPG Output pin ch.11 relocation 0
	SCK8_0		Multi-function Serial Clock I/O pin ch.8 relocation 0
52	VCC5	-	+5.0v Power Supply pin
53	VSS	-	GND pin
54	P037	I	General-Purpose I/O Port
	SEG23		LCDC Segment(Duty)Output pin
	ST0		LCDC Segment(Static)Output pin
	PPG12_0		PPG Output pin ch.12 relocation 0
	SIN7_0		LIN_UART Serial Input pin ch.7 relocation 0
55	P040	I	General-Purpose I/O Port
	SEG24		LCDC Segment(Duty)Output pin
	ST1		LCDC Segment(Static)Output pin
	PPG13_0		PPG Output pin ch.13 relocation 0
	SOT7_0		LIN_UART Serial Output pin ch.7 relocation 0

Pin Number	Pin Name	I/O Circuit Type	Function Description
56	P041	I	General-Purpose I/O Port
	SEG25		LCDC Segment(Duty)Output pin
	ST2		LCDC Segment(Static)Output pin
	PPG14_0		PPG Output pin ch.14 relocation 0
	SCK7_0		LIN_UART Serial Clock I/O pin ch.7 relocation 0
57	VCC5	-	+5.0v Power Supply pin
58	VSS	-	GND pin
59	P042	I	General-Purpose I/O Port
	SEG26		LCDC Segment(Duty)Output pin
	ST3		LCDC Segment(Static)Output pin
	PPG15_0		PPG Output pin ch.15 relocation 0
	AIN0_0		Up/down Counter AIN Input pin ch.0 relocation 0
60	P043	I	General-Purpose I/O Port
	SEG27		LCDC Segment(Duty)Output pin
	ST4		LCDC Segment(Static)Output pin
	BIN0_0		Up/down Counter BIN Input pin ch.0 relocation 0
	SGA4_0		Sound Generator SGA Output pin ch.4 relocation 0
	OCU6_1		Output Compare Output pin ch.6 relocation 1
61	P044	I	General-Purpose I/O Port
	SEG28		LCDC Segment(Duty)Output pin
	ST5		LCDC Segment(Static)Output pin
	ZIN0_0		Up/down Counter ZIN Input pin ch.0 relocation 0
	SGO4_0		Sound Generator SGO Output pin ch.4 relocation 0
	OCU7_1		Output Compare Output pin ch.7 relocation 1
62	P045	I	General-Purpose I/O Port
	SEG29		LCDC Segment(Duty)Output pin
	ST6		LCDC Segment(Static)Output pin
	AIN1_0		Up/down Counter AIN Input pin ch.1 relocation 0
	SIN8_2		Multi-function Serial Input pin ch.8 relocation 2
63	P046	I	General-Purpose I/O Port
	SEG30		LCDC Segment(Duty)Output pin
	ST7		LCDC Segment(Static)Output pin
	BIN1_0		Up/down Counter BIN Input pin ch.1 relocation 0
	SOT8_2		Multi-function Serial Output pin ch.8 relocation 2
64	P047	I	General-Purpose I/O Port
	SEG31		LCDC Segment(Duty)Output pin
	ST8		LCDC Segment(Static)Output pin
	ZIN1_0		Up/down Counter ZIN Input pin ch.1 relocation 0
	SCK8_2		Multi-function Serial Clock I/O pin ch.8 relocation 2
65	P050	I	General-Purpose I/O Port
	COM0		LCDC Segment(Duty)Common Output pin
	OCU8_1		Output Compare Output pin ch.8 relocation 1
66	P051	I	General-Purpose I/O Port
	COM1		LCDC Segment(Duty)Common Output pin
	OCU9_1		Output Compare Output pin ch.9 relocation 1
67	P052	I	General-Purpose I/O Port
	COM2		LCDC Segment(Duty)Common Output pin
	OCU10_1		Output Compare Output pin ch.10 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
68	P053	I	General-Purpose I/O Port
	COM3		LCDC Segment(Duty)Common Output pin
	OCU11_1		Output Compare Output pin ch.11 relocation 1
69	P054	I2	General-Purpose I/O Port
	V0		LCDC Reference Voltage V0 Input pin
	FRCK0_1		Free-Run Timer Clock Input pin ch.0 relocation 1
70	P055	I2	General-Purpose I/O Port
	V1		LCDC Reference Voltage V1 Input pin
	FRCK1_1		Free-Run Timer Clock Input pin ch.1 relocation 1
71	P056	I2	General-Purpose I/O Port
	V2		LCDC Reference Voltage V2 Input pin
	FRCK2_1		Free-Run Timer Clock Input pin ch.2 relocation 1
72	P057	I3	General-Purpose I/O Port
	V3		LCDC Reference Voltage V3 Input pin
	FRCK3_1		Free-Run Timer Clock Input pin ch.3 relocation 1
73	DVCC	-	Power Supply pin for SMC high current
74	DVSS	-	GND pin for SMC high current
75	P060	K	General-Purpose I/O Port
	PWM1P0		SMC Output pin ch.0
	AN8		ADC Analog Input pin ch.8
76	P061	K	General-Purpose I/O Port
	PWM1M0		SMC Output pin ch.0
	AN9		ADC Analog Input pin ch.9
	SIN1_1		Multi-function Serial Input pin ch.1 relocation 1
77	P062	K	General-Purpose I/O Port
77	PWM2P0	K	SMC Output pin ch.0
	AN10		ADC Analog Input pin ch.10
	SOT1_1		Multi-function Serial Output pin ch.1 relocation 1
	ZIN1_1		Up/down Counter ZIN Input pin ch.1 relocation 1
78	P063	K	General-Purpose I/O Port
	PWM2M0		SMC Output pin ch.0
	AN11		ADC Analog Input pin ch.11
	SCK1_1		Multi-function Serial Clock I/O pin ch.1 relocation 1
	BIN1_1		Up/down Counter BIN Input pin ch.1 relocation 1
79	P064	K	General-Purpose I/O Port
	PWM1P1		SMC Output pin ch.1
	AN12		ADC Analog Input pin ch.12
	SIN0_1		Multi-function Serial Input pin ch.0 relocation 1
	AIN1_1		Up/down Counter AIN Input pin ch.1 relocation 1
80	P065	K	General-Purpose I/O Port
	PWM1M1		SMC Output pin ch.1
	AN13		ADC Analog Input pin ch.13
	SOT0_1		Multi-function Serial Output pin ch.0 relocation 1
	ZIN0_1		Up/down Counter ZIN Input pin ch.0 relocation 1
81	P066	K	General-Purpose I/O Port
	PWM2P1		SMC Output pin ch.1
	AN14		ADC Analog Input pin ch.14
	SCK0_1		Multi-function Serial Clock I/O pin ch.0 relocation 1
	BIN0_1		Up/down Counter BIN Input pin ch.0 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
82	P067	K	General-Purpose I/O Port
	PWM2M1		SMC Output pin ch.1
	AN15		ADC Analog Input pin ch.15
	SIN9_1		Multi-function Serial Input pin ch.9 relocation 1
	AIN0_1		Up/down Counter AIN Input pin ch.0 relocation 1
83	DVCC	-	Power Supply pin for SMC high current
84	DVSS	-	GND pin for SMC high current
85	P070	K	General-Purpose I/O Port
	PWM1P2		SMC Output pin ch.2
	AN16		ADC Analog Input pin ch.16
	SOT9_1		Multi-function Serial Output pin ch.9 relocation 1
86	P071	K	General-Purpose I/O Port
	PWM1M2		SMC Output pin ch.2
	AN17		ADC Analog Input pin ch.17
	SCK9_1		Multi-function Serial Clock I/O pin ch.9 relocation 1
87	P072	K	General-Purpose I/O Port
	PWM2P2		SMC Output pin ch.2
	AN18		ADC Analog Input pin ch.18
	SIN8_1		Multi-function Serial Input pin ch.8 relocation 1
	ICU11_1		Input Capture Input pin ch.11 relocation 1
88	P073	K	General-Purpose I/O Port
	PWM2M2		SMC Output pin ch.2
	AN19		ADC Analog Input pin ch.19
	SOT8_1		Multi-function Serial Output pin ch.8 relocation 1
	ICU10_1		Input Capture Input pin ch.10 relocation 1
89	P074	K	General-Purpose I/O Port
	PWM1P3		SMC Output pin ch.3
	AN20		ADC Analog Input pin ch.20
	SCK8_1		Multi-function Serial Clock I/O pin ch.8 relocation 1
	ICU9_1		Input Capture Input pin ch.9 relocation 1
	PPG12_1		PPG Output pin ch.12 relocation 1
90	P075	K	General-Purpose I/O Port
	PWM1M3		SMC Output pin ch.3
	AN21		ADC Analog Input pin ch.21
	SIN7_1		LIN_UART Serial Input pin ch.7 relocation 1
	ICU8_1		Input Capture Input pin ch.8 relocation 1
	PPG13_1		PPG Output pin ch.13 relocation 1
91	P076	K	General-Purpose I/O Port
	PWM2P3		SMC Output pin ch.3
	AN22		ADC Analog Input pin ch.22
	SOT7_1		LIN_UART Serial Output pin ch.7 relocation 1
	ICU7_1		Input Capture Input pin ch.7 relocation 1
	PPG14_1		PPG Output pin ch.14 relocation 1
92	P077	K	General-Purpose I/O Port
	PWM2M3		SMC Output pin ch.3
	AN23		ADC Analog Input pin ch.23
	SCK7_1		LIN_UART Serial Clock I/O pin ch.7 relocation 1
	ICU6_1		Input Capture Input pin ch.6 relocation 1
	PPG15_1		PPG Output pin ch.15 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
93	DVCC	-	Power Supply pin for SMC high current
94	DVSS	-	GND pin for SMC high current
95	P080	K	General-Purpose I/O Port
	PWM1P4		SMC Output pin ch.4
	AN24		ADC Analog Input pin ch.24
	SIN6_0		LIN_UART Serial Input pin ch.6 relocation 0
	PPG16_0		PPG Output pin ch.16 relocation 0
	AIN0_2		Up/down Counter AIN Input pin ch.0 relocation 2
96	P081	K	General-Purpose I/O Port
	PWM1M4		SMC Output pin ch.4
	AN25		ADC Analog Input pin ch.25
	SOT6_0		LIN_UART Serial Output pin ch.6 relocation 0
	PPG17_0		PPG Output pin ch.17 relocation 0
	BIN0_2		Up/down Counter BIN Input pin ch.0 relocation 2
97	P082	K	General-Purpose I/O Port
	PWM2P4		SMC Output pin ch.4
	AN26		ADC Analog Input pin ch.26
	SCK6_0		LIN_UART Serial Clock I/O pin ch.6 relocation 0
	PPG18_0		PPG Output pin ch.18 relocation 0
	ZIN0_2		Up/down Counter ZIN Input pin ch.0 relocation 2
98	P083	K	General-Purpose I/O Port
	PWM2M4		SMC Output pin ch.4
	AN27		ADC Analog Input pin ch.27
	ICU0_2		Input Capture Input pin ch.0 relocation 2
	PPG19_0		PPG Output pin ch.19 relocation 0
99	P084	K	General-Purpose I/O Port
	PWM1P5		SMC Output pin ch.5
	AN28		ADC Analog Input pin ch.28
	ICU1_2		Input Capture Input pin ch.1 relocation 2
	PPG20_0		PPG Output pin ch.20 relocation 0
100	P085	K	General-Purpose I/O Port
	PWM1M5		SMC Output pin ch.5
	AN29		ADC Analog Input pin ch.29
	ICU2_2		Input Capture Input pin ch.2 relocation 2
	PPG21_0		PPG Output pin ch.21 relocation 0
101	P086	K	General-Purpose I/O Port
	PWM2P5		SMC Output pin ch.5
101	AN30	K	ADC Analog Input pin ch.30
	ICU3_2		Input Capture Input pin ch.3 relocation 2
	PPG22_0		PPG Output pin ch.22 relocation 0
102	P087	K	General-Purpose I/O Port
	PWM2M5		SMC Output pin ch.5
	AN31		ADC Analog Input pin ch.31
	ICU4_2		Input Capture Input pin ch.4 relocation 2
	PPG23_0		PPG Output pin ch.23 relocation 0
103	DVCC	-	Power Supply pin for SMC high current
104	DVSS	-	GND pin for SMC high current
105	Non connection	-	Non connection

Pin Number	Pin Name	I/O Circuit Type	Function Description
106	P090	M	General-Purpose I/O Port
	ADTG		ADC External Trigger Input pin
	PPG0_2		PPG Output pin ch.0 relocation 2
107	P100	J	General-Purpose I/O Port
	SIN4_1		LIN_UART Serial Input pin ch.4 relocation 1
	AN0		ADC Analog Input pin ch.0
	TIN0_1		Reload Timer Event Input pin ch.0 relocation 1
	PPG8_0		PPG Output pin ch.8 relocation 0
108	Non connection	-	Non connection
109	P101	J	General-Purpose I/O Port
	SOT4_1		LIN_UART Serial Output pin ch.4 relocation 1
	AN1		ADC Analog Input pin ch.1
	TIN1_1		Reload Timer Event Input pin ch.1 relocation 1
	PPG9_0		PPG Output pin ch.9 relocation 0
110	Non connection	-	Non connection
111	P102	J	General-Purpose I/O Port
	SCK4_1		LIN_UART Serial Clock I/O pin ch.4 relocation 1
	AN2		ADC Analog Input pin ch.2
	TIN2_1		Reload Timer Event Input pin ch.2 relocation 1
	PPG10_0		PPG Output pin ch.10 relocation 0
	ICU6_2		Input Capture Input pin ch.6 relocation 2
112	P103	J	General-Purpose I/O Port
	SIN5_1		LIN_UART Serial Input pin ch.5 relocation 1
	AN3		ADC Analog Input pin ch.3
	TIN3_1		Reload Timer Event Input pin ch.3 relocation 1
	PPG1_1		PPG Output pin ch.1 relocation 1
	ICU7_2		Input Capture Input pin ch.7 relocation 2
113	Non connection	-	Non connection
114	P104	J	General-Purpose I/O Port
	SOT5_1		LIN_UART Serial Output pin ch.5 relocation 1
	AN4		ADC Analog Input pin ch.4
	TOT0_1		Reload Timer Output pin ch.0 relocation 0
	PPG2_1		PPG Output pin ch.2 relocation 1
	ICU8_2		Input Capture Input pin ch.8 relocation 2
115	P105	J	General-Purpose I/O Port
	SCK5_1		LIN_UART Serial Clock I/O pin ch.5 relocation 1
	AN5		ADC Analog Input pin ch.5
	TOT1_1		Reload Timer Output pin ch.1 relocation 1
	PPG3_1		PPG Output pin ch.3 relocation 1
	ICU9_2		Input Capture Input pin ch.9 relocation 2
116	Non connection	-	Non connection
117	P106	J	General-Purpose I/O Port
	AN6		ADC Analog Input pin ch.6
	PPG4_1		PPG Output pin ch.4 relocation 1
117	ICU10_2	J	Input Capture Input pin ch.10 relocation 2
	SGA4_1		Sound Generator SGA Output pin ch.4 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
118	P107	L	General-Purpose I/O Port
	AN7		ADC Analog Input pin ch.7
	PPG5_1		PPG Output pin ch.5 relocation 1
	DAO1		DAC Output pin ch.1
	ICU11_2		Input Capture Input pin ch.11 relocation 2
	SGO4_1		Sound Generator SGO Output pin ch.4 relocation 1
119	Non connection	-	Non connection
120	AVSS	-	ADC, DAC GND pin
	AVRL		ADC Low Reference Voltage pin
121	AVRH	-	ADC High Reference Voltage pin
122	AVCC	-	ADC,DAC Analog Power Supply pin
123	Non connection	-	Non connection
124	P123	L	General-Purpose I/O Port
	OCU1_0		Output Compare Output pin ch.1 relocation 0
	PPG8_2		PPG Output pin ch.8 relocation 2
	DAO0		DAC Output pin ch.0
	AN39		ADC Analog Input pin ch.39
125	P122	J	General-Purpose I/O Port
	OCU0_0		Output Compare Output pin ch.0 relocation 0
	SCK5_0		LIN_UART Serial Clock I/O pin ch.5 relocation 0
	TOT3_0		Reload Timer Output pin ch.3 relocation 0
	PPG7_2		PPG Output pin ch.7 relocation 2
	AN38		ADC Analog Input pin ch.38
126	P121	J	General-Purpose I/O Port
	FRCK0_0		Free-Run Timer Clock Input pin ch.0 relocation 0
	SOT5_0		LIN_UART Serial Output pin ch.5 relocation 0
	INT7_0		External Interrupt Request Input pin ch.7 relocation 0
	TOT2_0		Reload Timer Output pin ch.2 relocation 0
	PPG6_2		PPG Output pin ch.6 relocation 2
	AN37		ADC Analog Input pin ch.37
127	P120	J	General-Purpose I/O Port
	FRCK1_0		Free-Run Timer Clock Input pin ch.1 relocation 0
	SIN5_0		LIN_UART Serial Input pin ch.5 relocation 0
	INT6_0		External Interrupt Request Input pin ch.6 relocation 0
	TOT1_0		Reload Timer Output pin ch.1 relocation 0
	PPG5_2		PPG Output pin ch.5 relocation 2
	AN36		ADC Analog Input pin ch.36
128	P117	J	General-Purpose I/O Port
	SCK4_0		LIN_UART Serial Clock I/O pin ch.4 relocation 0
	TOT0_0		Reload Timer Output pin ch.0 relocation 0
	SGO3		Sound Generator SGO Output pin ch.3
	FRCK2_0		Free-Run Timer Clock Input pin ch.2 relocation 0
	AN35		ADC Analog Input pin ch.35
	TRG4		PPG Trigger Input pin 4 (ch.16-ch.19)
129	P116	J	General-Purpose I/O Port
	SOT4_0		LIN_UART Serial Output pin ch.4 relocation 0
	TIN3_0		Reload Timer Event Input pin ch.3 relocation 0
	SGA3		Sound Generator SGA Output pin ch.3
	FRCK3_0		Free-Run Timer Clock Input pin ch.3 relocation 0
	AN34		ADC Analog Input pin ch.34

Pin Number	Pin Name	I/O Circuit Type	Function Description
130	P115	J	General-Purpose I/O Port
	SIN4_0		LIN_UART Serial Input pin ch.4 relocation 0
	TIN2_0		Reload Timer Event Input pin ch.2 relocation 0
130	SGO2	J	Sound Generator SGO Output pin ch.2
	FRCK4_0		Free-Run Timer Clock Input pin ch.4 relocation 0
	AN33		ADC Analog Input pin ch.33
131	P114	J	General-Purpose I/O Port
	SCK3_0		LIN_UART Serial Clock I/O pin ch.3 relocation 0
	TIN1_0		Reload Timer Event Input pin ch.1 relocation 0
	ICU5_1		Input Capture Input pin ch.5 relocation 1
	SGA2		Sound Generator SGA Output pin ch.2
	AN32		ADC Analog Input pin ch.32
	TRG3		PPG Trigger Input pin 3 (ch.12-ch.15)
132	P000	M	General-Purpose I/O Port
	SIN2_1		LIN_UART Serial Input pin ch.2 relocation 1
	TIN0_2		Reload Timer Event Input pin ch.0 relocation 2
	PPG0_0		PPG Output pin ch.0 relocation 0
	INT0_1		External Interrupt Request Input pin ch.0 relocation 1
133	P001	M	General-Purpose I/O Port
	SOT2_1		LIN_UART Serial Output pin ch.2 relocation 1
	TIN1_2		Reload Timer Event Input pin ch.1 relocation 2
	PPG1_0		PPG Output pin ch.1 relocation 0
	INT1_1		External Interrupt Request Input pin ch.1 relocation 1
134	P002	M	General-Purpose I/O Port
	SCK2_1		LIN_UART Serial Clock I/O pin ch.2 relocation 1
	TIN2_2		Reload Timer Event Input pin ch.2 relocation 2
	PPG2_0		PPG Output pin ch.2 relocation 0
	INT2_1		External Interrupt Request Input pin ch.2 relocation 1
135	P003	M	General-Purpose I/O Port
	SIN3_1		LIN_UART Serial Input pin ch.3 relocation 1
	TIN3_2		Reload Timer Event Input pin ch.3 relocation 2
	PPG3_0		PPG Output pin ch.3 relocation 0
	INT3_1		External Interrupt Request Input pin ch.3 relocation 1
136	VCC5	-	+5.0v Power Supply pin
137	VSS	-	GND pin
138	P137	M(Y)	General-Purpose I/O Port
	(X0A)		Sub Clock oscillation Input pin (only dual clock product)
139	P136	M(Y)	General-Purpose I/O Port
	(X1A)		Sub Clock oscillation Output pin (only dual clock product)
140	NMIX	R	NMI Pin
141	P004	M	General-Purpose I/O Port
	SOT3_1		LIN_UART Serial Output pin ch.3 relocation 1
	TOT0_2		Reload Timer Output pin ch.0 relocation 2
	PPG4_0		PPG Output pin ch.4 relocation 0
	INT4_1		External Interrupt Request Input pin ch.4 relocation 1
142	P005	M	General-Purpose I/O Port
	SCK3_1		LIN_UART Serial Clock I/O pin ch.3 relocation 1
	TOT1_2		Reload Timer Output pin ch.1 relocation 2
	PPG5_0		PPG Output pin ch.5 relocation 0
	INT5_1		External Interrupt Request Input pin ch.5 relocation 1

Pin Number	Pin Name	I/O Circuit Type	Function Description
143	P006	M	General-Purpose I/O Port
	TOT2_2		Reload Timer Output pin ch.2 relocation 2
	PPG6_0		PPG Output pin ch.6 relocation 0
	INT6_1		External Interrupt Request Input pin ch.6 relocation 1
144	P007	M	General-Purpose I/O Port
	TOT3_2		Reload Timer Output pin ch.3 relocation 2
	PPG7_0		PPG Output pin ch.7 relocation 0
	INT7_1		External Interrupt Request Input pin ch.7 relocation 1
145	Non connection	-	Non connection
146	P097	M	General-Purpose I/O Port
	WOT		RTC Overflow Output pin
	SOT3_0		LIN_UART Serial Output pin ch.3 relocation 0
	INT8_0		External Interrupt Request Input pin ch.8 relocation 0
	TIN0_0		Reload Timer Event Input pin ch.0 relocation 0
	ICU4_1		Input Capture Input pin ch.4 relocation 1
	PPG0_1		PPG Output pin ch.0 relocation 1
147	P094	M	General-Purpose I/O Port
	SGO1		Sound Generator SGO Output pin ch.1
	SIN3_0		LIN_UART Serial Input pin ch.3 relocation 0
	INT15_0		External Interrupt Request Input pin ch.15 relocation 0
	ICU1_1		Input Capture Input pin ch.1 relocation 1
	PPG9_1		PPG Output pin ch.9 relocation 1
148	P093	M	General-Purpose I/O Port
	SGA1		Sound Generator SGA Output pin ch.1
	SOT2_0		LIN_UART Serial Output pin ch.2 relocation 0
	INT14_0		External Interrupt Request Input pin ch.14 relocation 0
	ICU3_1		Input Capture Input pin ch.3 relocation 1
	PPG8_1		PPG Output pin ch.8 relocation 1
149	P092	M	General-Purpose I/O Port
	SGO0		Sound Generator SGO Output pin ch.0
	SCK2_0		LIN_UART Serial Clock I/O pin ch.0 relocation 0
	INT13_0		External Interrupt Request Input pin ch.13 relocation 0
	TOT3_1		Reload Timer Output pin ch.3 relocation 1
	ICU0_1		Input Capture Input pin ch.0 relocation 1
	PPG7_1		PPG Output pin ch.7 relocation 1
150	P091	M	General-Purpose I/O Port
	SGA0		Sound Generator SGA Output pin ch.0
	SIN2_0		LIN_UART Serial Input pin ch.2 relocation 0
	INT12_0		External Interrupt Request Input pin ch.12 relocation 0
	TOT2_1		Reload Timer Output pin ch.2 relocation 1
	ICU2_1		Input Capture Input pin ch.2 relocation 1
	PPG6_1		PPG Output pin ch.6 relocation 1
151	P110	M	General-Purpose I/O Port
	TX1		CAN TX Data Output pin ch.1
	PPG1_2		PPG Output pin ch.1 relocation 2
	FRCK5_0		Free-Run Timer Clock Input pin ch.5 relocation 0
152	P111	M	General-Purpose I/O Port
	RX1		CAN RX Data Input pin ch.1
	INT10_0		External Interrupt Request Input pin ch.10 relocation 0
	PPG2_2		PPG Output pin ch.2 relocation 2

Pin Number	Pin Name	I/O Circuit Type	Function Description
153	P112	M	General-Purpose I/O Port
	TX2		CAN TX Data Output pin ch.2
	PPG3_2		PPG Output pin ch.3 relocation 2
154	P113	M	General-Purpose I/O Port
	RX2		CAN RX Data Input pin ch.2
	INT11_0		External Interrupt Request Input pin ch.11 relocation 0
	PPG4_2		PPG Output pin ch.4 relocation 2
155	RSTX	R	Reset Pin
156	VCC5	-	+5.0v Power Supply pin
157	VSS	-	GND pin
158	DEBUGIF	B	DEBUG I/F pin
159	P095	M	General-Purpose I/O Port
	TX0		CAN TX Data Output pin ch.0
	PPG10_1		PPG Output pin ch.10 relocation 1
160	P096	M	General-Purpose I/O Port
	RX0		CAN RX Data Input pin ch.0
	INT9_0		External Interrupt Request Input pin ch.9 relocation 0
161	P124	M	General-Purpose I/O Port
	OCU2_0		Output Compare Output pin ch.2 relocation 0
	ICU5_2		Input Capture Input pin ch.5 relocation 2
	PPG9_2		PPG Output pin ch.9 relocation 2
162	Non connection	-	Non connection
163	Non connection	-	Non connection
164	Non connection	-	Non connection
165	Non connection	-	Non connection
166	MD0	A	Mode Pin 0
167	MD1	A	Mode Pin 1
168	MD2	R2	Mode Pin 2
169	X0	X	Main Clock oscillation Input pin
170	X1	X	Main Clock oscillation Output pin
171	VSS	-	GND pin
172	P125	M	General-Purpose I/O Port
	OCU3_0		Output Compare Output pin ch.3 relocation 0
	ICU0_0		Input Capture Input pin ch.0 relocation 0
	PPG10_2		PPG Output pin ch.10 relocation 2
173	P126	M	General-Purpose I/O Port
	TRG0		PPG Trigger Input pin 0 (ch.0-ch.3)
	SIN0_0		Multi-function Serial Input pin ch.0 relocation 0
	INT1_0		External Interrupt Request Input pin ch.1 relocation 0
	OCU4_0		Output Compare Output pin ch.4 relocation 0
174	P127	N	General-Purpose I/O Port
	SOT0_0		Multi-function Serial Output pin ch.0 relocation 0
	OCU5_0		Output Compare Output pin ch.5 relocation 0
175	P130	N	General-Purpose I/O Port
	SCK0_0		Multi-function Serial Clock I/O pin ch.0 relocation 0
	INT0_0		External Interrupt Request Input pin ch.0 relocation 0
	ICU1_0		Input Capture Input pin ch.1 relocation 0
	TIOA0		Base Timer I/O pin ch.0

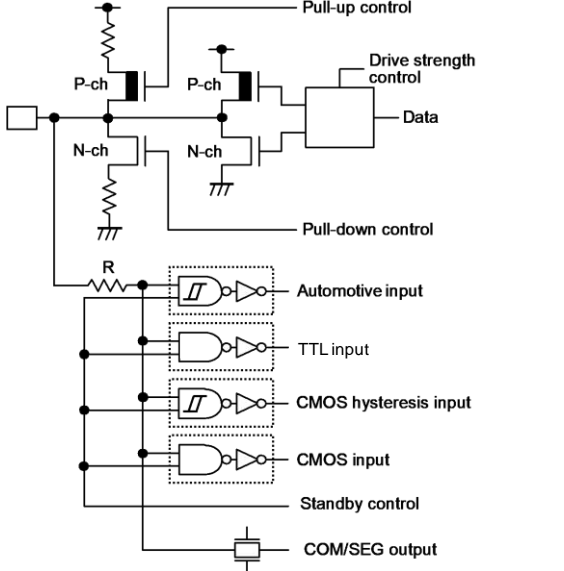
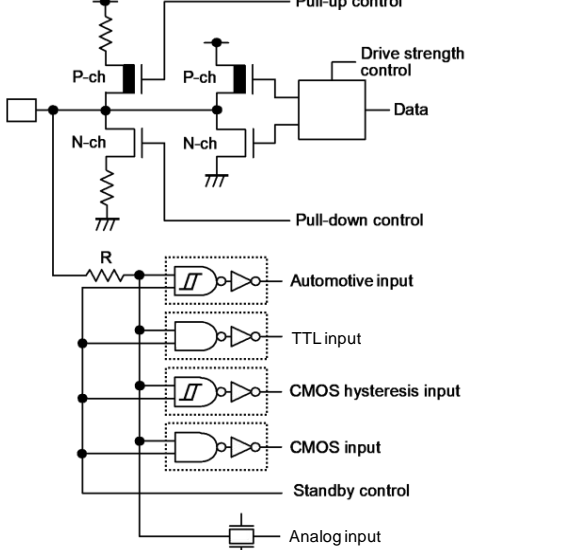
Pin Number	Pin Name	I/O Circuit Type	Function Description
176	P131	M	General-Purpose I/O Port
	TRG1		PPG Trigger Input pin 1 (ch.4-ch.7)
	SIN1_0		Multi-function Serial Input pin ch.1 relocation 0
	INT4_0		External Interrupt Request Input pin ch.4 relocation 0
	ICU2_0		Input Capture Input pin ch.2 relocation 0
	TIOA1		Base Timer I/O pin ch.1
177	P132	N	General-Purpose I/O Port
	SOT1_0		Multi-function Serial Output pin ch.1 relocation 0
	INT2_0		External Interrupt Request Input pin ch.2 relocation 0
	ICU3_0		Input Capture Input pin ch.3 relocation 0
	TIOB0		Base Timer I/O pin ch.0
178	P133	N	General-Purpose I/O Port
	SCK1_0		Multi-function Serial Clock I/O pin ch.1 relocation 0
	INT3_0		External Interrupt Request Input pin ch.3 relocation 0
	ICU4_0		Input Capture Input pin ch.4 relocation 0
	TIOB1		Base Timer I/O pin ch.1
	TRG5		PPG Trigger Input pin 5 (ch.20-ch.23)
	PPG11_1		PPG Output pin ch.11 relocation 1
179	P134	M	General-Purpose I/O Port
	TRG2		PPG Trigger Input pin 2 (ch.8-ch.11)
	INT5_0		External Interrupt Request Input pin ch.5 relocation 0
	ICU5_0		Input Capture Input pin ch.5 relocation 0
	PPG1_3		PPG Output pin ch.1 relocation 3
180	VCC5	-	+5.0v Power Supply pin
181	VSS	-	GND pin
182	C	-	External Capacitance Connection Pin
183	P140	M2	General-Purpose I/O Port
	D16_0		External Bus Data I/O pin
	D24_1		External Bus Data I/O pin
184	P141	M2	General-Purpose I/O Port
	D17_0		External Bus Data I/O pin
	D25_1		External Bus Data I/O pin
185	P142	M2	General-Purpose I/O Port
	D18_0		External Bus Data I/O pin
	D26_1		External Bus Data I/O pin
186	P143	M2	General-Purpose I/O Port
	D19_0		External Bus Data I/O pin
	D27_1		External Bus Data I/O pin
187	P144	M2	General-Purpose I/O Port
	D20_0		External Bus Data I/O pin
	D28_1		External Bus Data I/O pin
188	P145	M2	General-Purpose I/O Port
	D21_0		External Bus Data I/O pin
	D29_1		External Bus Data I/O pin
189	P146	M2	General-Purpose I/O Port
	D22_0		External Bus Data I/O pin
	D30_1		External Bus Data I/O pin
190	P147	M2	General-Purpose I/O Port
	D23_0		External Bus Data I/O pin
	D31_1		External Bus Data I/O pin

Pin Number	Pin Name	I/O Circuit Type	Function Description
191	P150	M2	General-Purpose I/O Port
	D24_0		External Bus Data I/O pin
	D16_1		External Bus Data I/O pin
192	P151	M2	General-Purpose I/O Port
	D25_0		External Bus Data I/O pin
	D17_1		External Bus Data I/O pin
193	P152	M2	General-Purpose I/O Port
	D26_0		External Bus Data I/O pin
	D18_1		External Bus Data I/O pin
194	P153	M2	General-Purpose I/O Port
	D27_0		External Bus Data I/O pin
	D19_1		External Bus Data I/O pin
195	P154	M2	General-Purpose I/O Port
	D28_0		External Bus Data I/O pin
	D20_1		External Bus Data I/O pin
196	P155	M2	General-Purpose I/O Port
	D29_0		External Bus Data I/O pin
	D21_1		External Bus Data I/O pin
197	P156	M2	General-Purpose I/O Port
	D30_0		External Bus Data I/O pin
	D22_1		External Bus Data I/O pin
198	P157	M2	General-Purpose I/O Port
	D31_0		External Bus Data I/O pin
	D23_1		External Bus Data I/O pin
199	P160	M2	General-Purpose I/O Port
	ASX		External Bus Address-Strobe Output pin
200	P161	M2	General-Purpose I/O Port
	CS0X		External Bus Chip-Select 0 Output pin
201	P162	M2	General-Purpose I/O Port
	CS1X		External Bus Chip-Select 1 Output pin
202	P163	M2	General-Purpose I/O Port
	RDX		External Bus Read-Strobe Output pin
203	P164	M2	General-Purpose I/O Port
	WROX		External Bus Write-Strobe 0 Output pin
204	P165	M2	General-Purpose I/O Port
	WR1X		External Bus Write-Strobe 1 Output pin
205	P166	M2	General-Purpose I/O Port
	A00		External Bus Address Output pin
206	P167	M2	General-Purpose I/O Port
	A01		External Bus Address Output pin
207	P170	M2	General-Purpose I/O Port
	A02		External Bus Address Output pin
208	VSS	-	GND pin

6. I/O Circuit Type

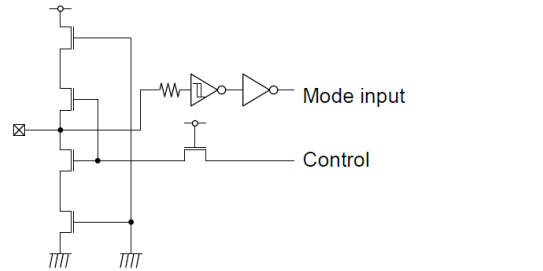
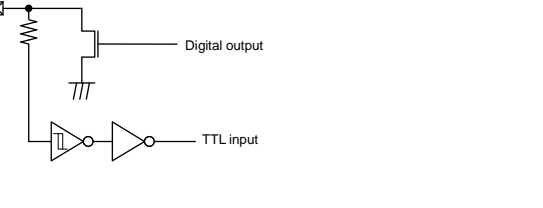
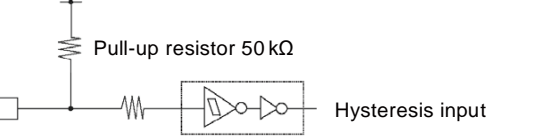
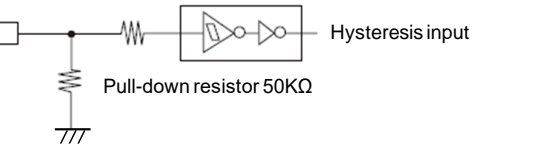
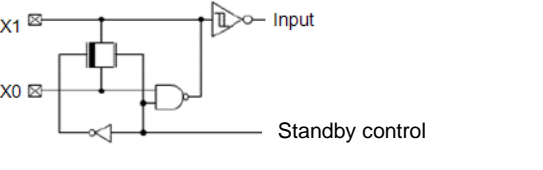
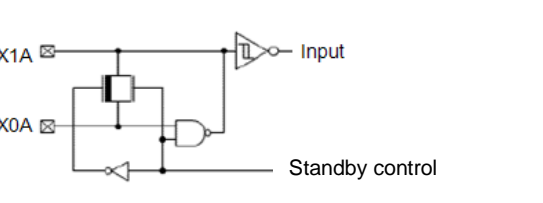
Type	Circuit	Remarks
H		<p>General-purpose I/O port with COM/SEG output and with against 3V pad power supply (5V tolerant).</p> <p>IOH = -1/-2 mA (@VCCE = 5 V), IOH = -0.5/-1/-2 mA (@VCCE = 3.3 V), IOL = 1/2 mA (@VCCE = 5 V), IOL = 0.5/1/2 mA (@VCCE = 3.3 V)</p> <p>Pull-down resistor control Automotive level input TTL level input CMOS level hysteresis input CMOS level input</p>
I		<p>General-purpose I/O port with COM/SEG output.</p> <p>IOH = -1/-2 mA, IOL = 1/2 mA</p> <p>Pull-up resistor control Pull-down resistor control Automotive level input TTL level input CMOS level hysteresis input CMOS level input</p>

Type	Circuit	Remarks
I2		<p>General-purpose I/O port with LCDC reference voltage input</p> <p>IOH = -1/-2 mA, IOL = 1/2 mA</p> <p>Pull-up resistor control</p> <p>Pull-down resistor control</p> <p>Automotive level input</p> <p>TTL level input</p> <p>CMOS level hysteresis input</p> <p>CMOS level input</p>
I3		<p>General-purpose input port with LCDC V3 input</p> <p>Pull-up resistor control</p> <p>Pull-down resistor control</p> <p>Automotive level input</p> <p>TTL level input</p> <p>CMOS level hysteresis input</p> <p>CMOS level input</p>

Type	Circuit	Remarks
I4		<p>General-purpose I/O port with COM/SEG output.</p> <p>IOH = -1/-2 mA(@VCCE = 5 V), IOH = -0.5/-1 mA(@VCCE = 3.3 V), IOL = 1/2 mA(@VCCE = 5 V), IOL = 0.5/1 mA(@VCCE = 3.3 V)</p> <p>Pull-up resistor control Pull-down resistor control Automotive level input TTL level input CMOS level hysteresis input CMOS level input</p>
J		<p>General-purpose I/O port with analog input.</p> <p>IOH = -1/-2 mA, IOL = 1/2 mA</p> <p>Pull-up resistor control Pull-down resistor control Automotive level input TTL level input CMOS level hysteresis input CMOS level input</p>

Type	Circuit	Remarks
K		<p>General-purpose I/O port with analog input and with high current capable for SMC.</p> <p>$IOH = -1/-2/-30\text{ mA}$, $IOL = 1/2/30\text{ mA}$</p> <p>Pull-up resistor control</p> <p>Pull-down resistor control</p> <p>Automotive level input</p> <p>TTL level input</p> <p>CMOS level hysteresis input</p> <p>CMOS level input</p>
L		<p>General-purpose I/O port with analog input and with DAC output</p> <p>$IOH = -1/-2\text{ mA}$, $IOL = 1/2\text{ mA}$</p> <p>Pull-up resistor control</p> <p>Pull-down resistor control</p> <p>Automotive level input</p> <p>TTL level input</p> <p>CMOS level hysteresis input</p> <p>CMOS level input</p>

Type	Circuit	Remarks
M		<p>General-purpose I/O port.</p> <p>$I_{OH} = -1/-2$ mA, $I_{OL} = 1/2$ mA</p> <p>Pull-up resistor control</p> <p>Pull-down resistor control</p> <p>Automotive level input</p> <p>TTL level input</p> <p>CMOS level hysteresis input</p> <p>CMOS level input</p>
M2		<p>General-purpose I/O port.</p> <p>$I_{OH} = -1/-2$ mA (@ $V_{CC} = 5$ V), $I_{OH} = -0.5/-1$ mA (@ $V_{CC} = 3.3$ V), $I_{OL} = 1/2$ mA (@ $V_{CC} = 5$ V), $I_{OL} = 0.5/1$ mA (@ $V_{CC} = 3.3$ V)</p> <p>Pull-up resistor control</p> <p>Pull-down resistor control</p> <p>Automotive level input</p> <p>TTL level input</p> <p>CMOS level hysteresis input</p> <p>CMOS level input</p>
N		<p>General-purpose I/O port with I²C output</p> <p>$I_{OH} = -1/-2/-3$ mA, $I_{OL} = 1/2/3$ mA</p> <p>Pull-up resistor control</p> <p>Pull-down resistor control</p> <p>Automotive level input</p> <p>TTL level input</p> <p>CMOS level hysteresis input</p> <p>CMOS level input</p>

Type	Circuit	Remarks
A		Mode pin
B		DEBUG I/F pin
R		CMOS level hysteresis input
R2		CMOS level hysteresis input
X		Main oscillation I/O
Y		Sub oscillation I/O

7. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

7.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high-voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

7.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

7.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity
Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity
When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil
Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation
Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame
CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

8. Handling Devices

This section explains the latch-up prevention and the treatment of a pin.

For Latch-up Prevention

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC pin and VSS pin, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply voltage (AVcc, AVRH), analog input, and the power supply voltage to high-current output buffer pins (DVcc), the power supply voltage of external bus interface (VccE) must not exceed the digital power supply voltage (Vcc5) when the power supply voltage to the analog system and high-current output buffer pins the power supply voltage of external bus interface (VccE) is turned on or off.

In the correct power-on sequence, turn on the digital power supply voltage (Vcc5), analog power supply voltage (AVcc, AVRH), the power supply voltage of external bus interface (VccE), and the power supply voltage of high-current output buffer pins (DVcc) simultaneously. Or, turn on the digital power supply voltage (Vcc5), and then turn on analog power supply voltage (AVcc, AVRH), the power supply voltage of external bus interface (VccE), and the power supply voltage of high-current output buffer pins (DVcc).

Treatment of Unused Pins

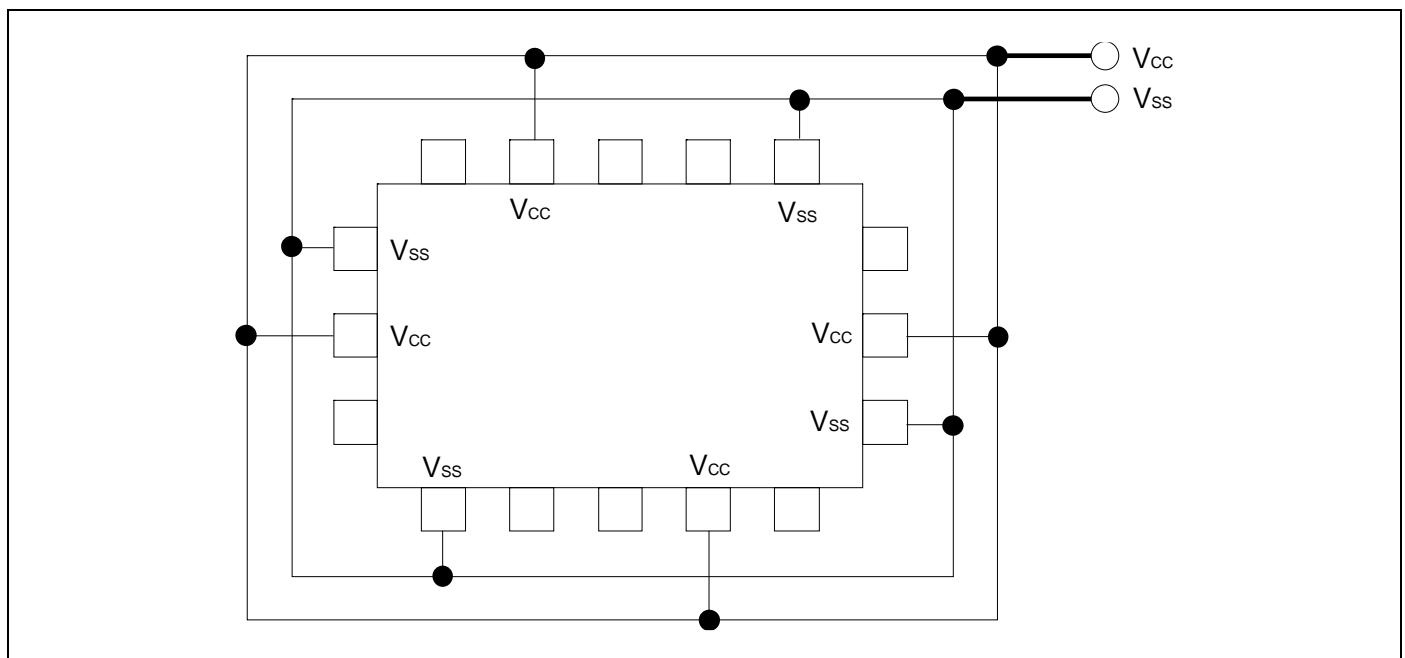
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect a 2kΩ resistor to each of unused pins for pull-up or pull-down connection.

Also, if I/O pins are not used, they must be set to the output state for opening or they must be set to the input state and treated in the same way as for the input pins.

Power Supply Pins

The device is designed to ensure that if the device contains multiple VCC pin or VSS pin, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power source or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1. Power Supply Input Pins



The power supply pins should be connected to VCC pin and VSS pin of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between the VCC pin and the VSS pin.

Crystal Oscillation Circuit

An external noise to the X0 pin or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out the X0 pin and the X1 pin, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 pin and X1 pin by ground circuits.

Mode Pins (MD2, MD1, MD0)

Connect the MD2, MD1 and MD0 mode pin to the VCC pin or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC pin or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

During Power-on

To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50 μ s or longer (between 0.2V to 2.7V) during power-on.

Notes During PLL Clock Operation

When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

Treatment of A/D Converter Power Supply Pins

Connect the pins to have $AV_{CC} = AVR_{H} = V_{CC5}$ and $AV_{SS}/AV_{RL} = V_{SS}$ even if the A/D converter is not used.

Notes on Using External Clock

An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

Power-on Sequence of A/D Converter Analog Inputs

Be sure to turn on the digital power supply voltage (V_{CC}) first, and then turn on the A/D converter power supply voltage (AV_{CC} , AVR_{H} , AVR_{L}) and analog input voltage ($AN0$ to $AN39$). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply voltage (V_{CC5}). When the AVR_{H} pin voltage is turned on or off, it must not exceed AV_{CC} . Even if a common analog input pin is used as an input port, its input voltage must not exceed AV_{CC} . (However, the analog power supply voltage and digital power supply voltage can be turned on or off simultaneously.)

Treatment of Power Supplies for High Current Output Buffer Pins (DV_{CC} , DV_{SS})

Be sure to turn on the digital power supply voltage (V_{CC}) first, and then turn on the power supply voltage for high current output buffer pins (DV_{CC} , DV_{SS}). Also, turn off the power supplies for high current output buffer pins first, and then turn off the digital power supply voltage (V_{CC}).

Even if the high current output buffer pins are used as general-purpose ports, the power supply voltage of high current output buffer pins (DV_{CC} , DV_{SS}) must be powered. (The power supplies of high current output buffer pins and the digital power supplies can be turned on or off simultaneously.)

Treatment of C Pin

This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device.

For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

Function Switching of a Multiplexed Port

To switch between the port function and the multiplexed pin function, use the PFR (port function register). However, if a pin is also used for an external bus, its function is switched by the external bus setting. For details, see "I/O Ports".

Low-power Consumption Mode

To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in the "Activating the sleep mode, watch mode, or stop mode" or the "Activating the watch mode (power-off) or stop mode(power-off)" of "POWER CONSUMPTION CONTROL" in Hardware Manual.

Take the following notes when using a monitor debugger.

- Do not set a break point for the low-power consumption transition program.
- Do not execute an operation step for the low-power consumption transition program.

Precautions When Writing to Registers Including the Status Flag

When writing a function control data in the register that has a status flag (especially, an interrupt request flag), taking care not to clear its status flag erroneously must be followed.

The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

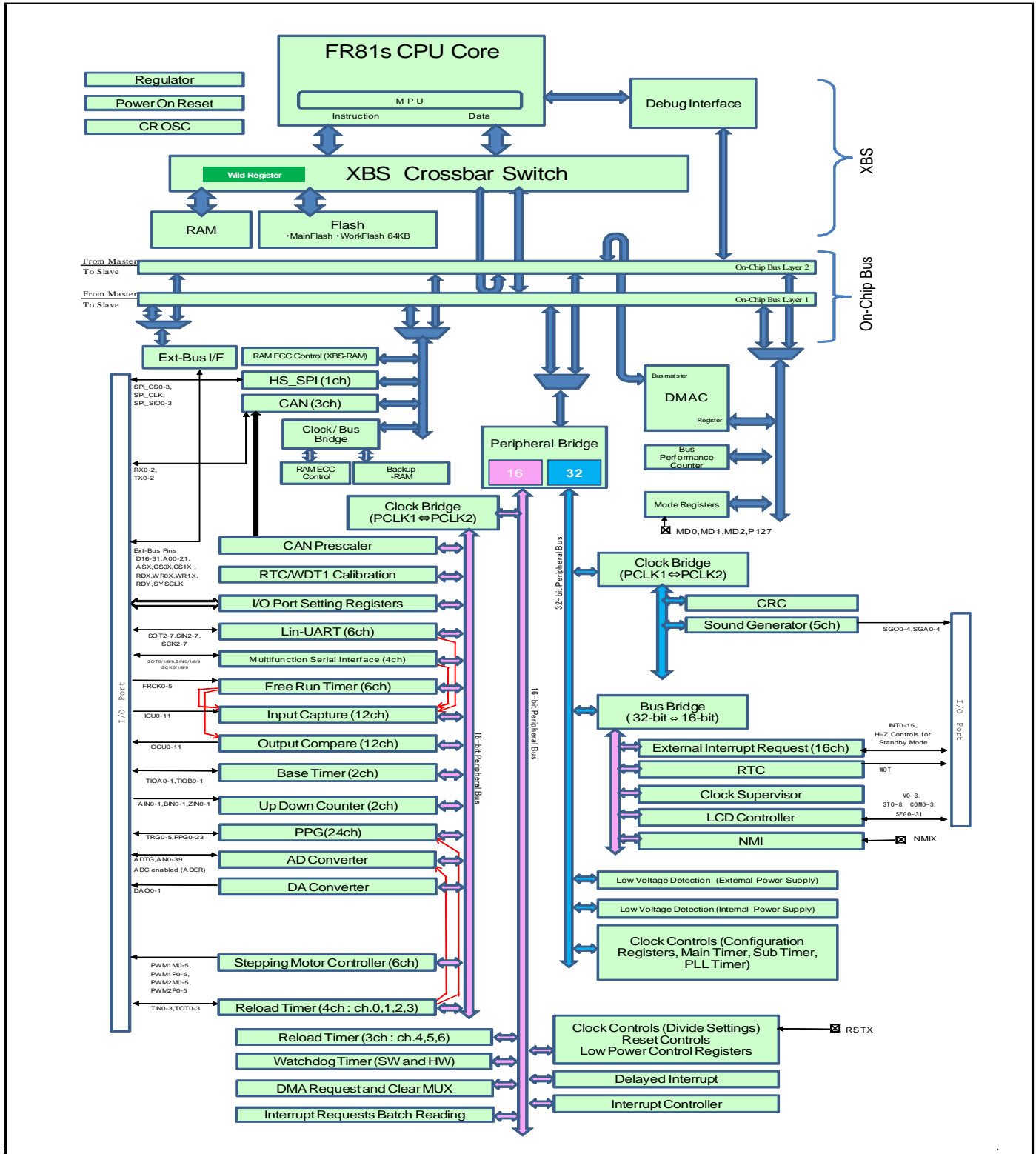
Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, writing data in the control bits and status flag simultaneously is done. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

Note: These points can be ignored because the bit instructions to a register which supports RMW are already taken the points into consideration. Care must be taken when the bit instruction is used to a register which does not support RMW.

No-connected-pin

The product of LQFP-208 has some no-connected-pin which is not connected to any function on die. Pins are recommended to be pulled-up or pulled-down on the extern circuit.

9. Block Diagram



Note: In this series, the HS-SPI function is prohibited

10. Memory Map

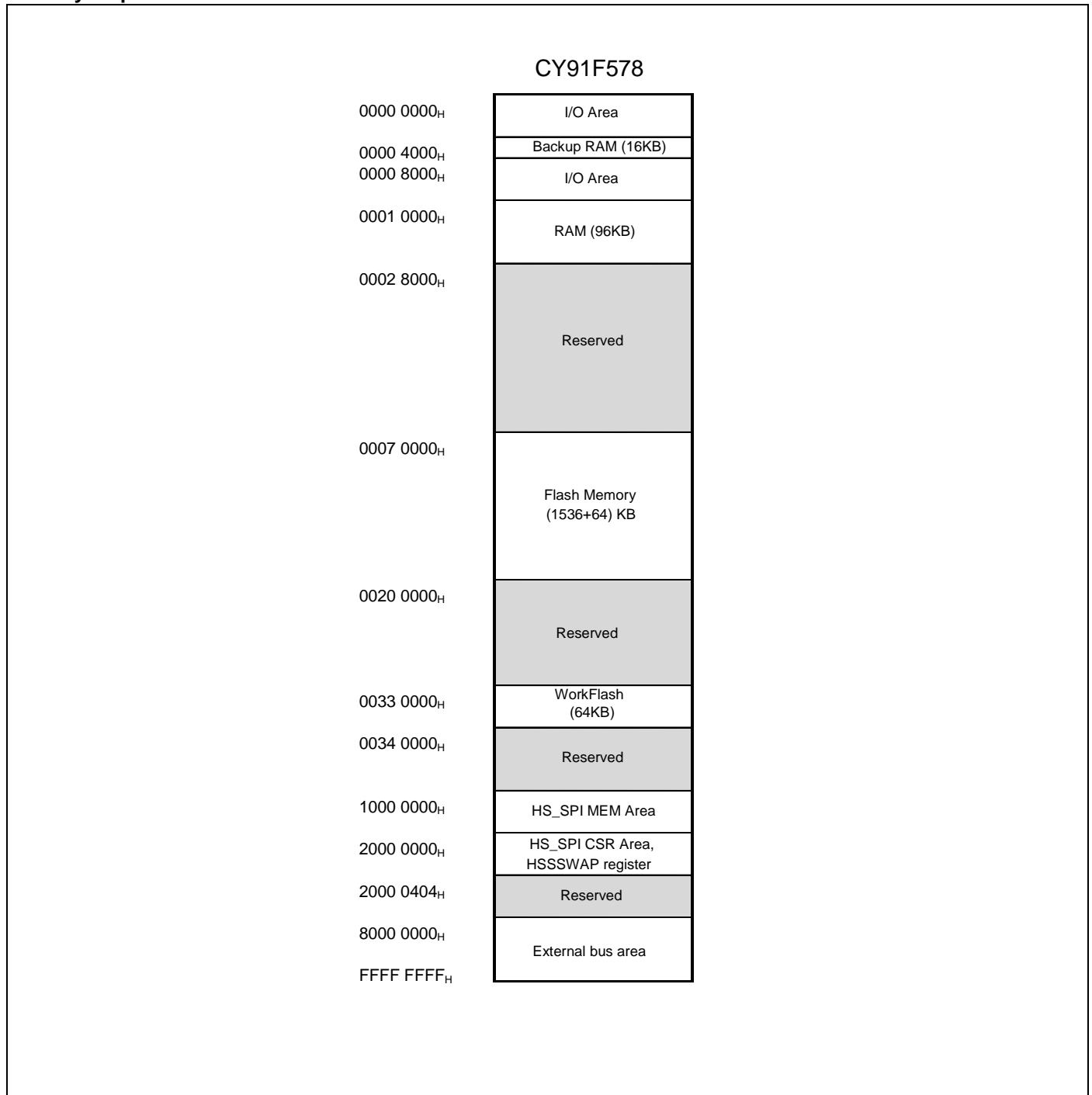
Memory Map

CY91F575	
0000 0000 _H	I/O Area
0000 4000 _H	BackUp RAM (8KB)
0000 6000 _H	I/O Area
0001 0000 _H	RAM (40KB)
0001 A000 _H	Reserved
0007 0000 _H	Flash memory (512+64)KB
0010 0000 _H	Reserved
0033 0000 _H	WorkFlash (64KB)
0034 0000 _H	Reserved
1000 0000 _H	HS_SPI MEM Area
2000 0000 _H	HS_SPI CSR area
2000 0404 _H	HSSSWAP register
	Reserved
8000 0000 _H	
FFFF FFFF _H	External bus Area

Memory Map

CY91F577	
0000 0000 _H	I/O Area
0000 4000 _H	Backup RAM (8KB)
0000 6000 _H	I/O Area
0001 0000 _H	RAM (64KB)
0002 0000 _H	Reserved
0007 0000 _H	Flash Memory (1024+64) KB
0018 0000 _H	Reserved
0033 0000 _H	WorkFlash (64KB)
0034 0000 _H	Reserved
1000 0000 _H	HS_SPI MEM Area
2000 0000 _H	HS_SPI CSR Area, HSSSWAP register
2000 0404 _H	Reserved
8000 0000 _H	External bus area
FFFF FFFF _H	

Memory Map



Memory Map

CY91F579	
0000 0000 _H	I/O Area
0000 4000 _H	Backup RAM (16KB)
0000 8000 _H	I/O Area
0001 0000 _H	RAM (128KB)
0003 0000 _H	Reserved
0007 0000 _H	Flash Memory (2048+64) KB
0028 0000 _H	Reserved
0033 0000 _H	WorkFlash (64KB)
0034 0000 _H	Reserved
1000 0000 _H	HS_SPI MEM Area
2000 0000 _H	HS_SPI CSR Area, HSSSWAP register
2000 0404 _H	Reserved
8000 0000 _H	External bus area
FFFF FFFF _H	

11. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map

Read/Write attribute (R: Read W: Write)

Address	Address offset value/ register name				Block
	+0	+1	+2	+3	
000090 _H	BTITMR[R] H 0000000000000000		BTITMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094 _H	—	BT1STC[R/W] B 00000000	—	—	
000098 _H	BT1PCSR/BT1PRL[R/W] H 0000000000000000		BT1PDU T/BT1PRLH/BT1D TBF[R/W] H 0000000000000000		
00009C _H	BTSEL[R/W] B ---0000	—	BTSSSR[W] B,H -----11		
0000A0 _H	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		A/D converter
0000A4 _H	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ----XX	ADCR0 [R] B, H,W XXXXX XXX	
0000A8 _H	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

Data access attribute
B: Byte
H: Half-word
W: Word

(Note)
The access by the data access attribute not described is disabled.

Initial register value after reset

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- **": Initial value "0" or "1" according to the setting

Note:

It is prohibited to access addresses not described here.

Table: I/O Map

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000000 _H	PDR00[R/W] B,H,W XXXXXXXX	PDR01[R/W] B,H,W XXXXXXXX	PDR02[R/W] B,H,W XXXXXXXX	PDR03[R/W] B,H,W XXXXXXXX	Port data register *4:CY91F578/9 only
000004 _H	PDR04[R/W] B,H,W XXXXXXXX	PDR05[R/W] B,H,W XXXXXXXX	PDR06[R/W] B,H,W XXXXXXXX	PDR07[R/W] B,H,W XXXXXXXX	
000008 _H	PDR08[R/W] B,H,W XXXXXXXX	PDR09[R/W] B,H,W XXXXXXXX	PDR10[R/W] B,H,W XXXXXXXX	PDR11[R/W] B,H,W XXXXXXXX	
00000C _H	PDR12[R/W] B,H,W XXXXXXXX	PDR13[R/W] B,H,W XX-XXXX	PDR14[R/W] B,H,W XXXXXXXX ^{*4}	PDR15[R/W] B,H,W XXXXXXXX ^{*4}	
000010 _H	PDR16[R/W] B,H,W XXXXXXXX ^{*4}	PDR17[R/W] B,H,W XXXXXXXX ^{*4}	PDR18[R/W] B,H,W XXXXXXXX ^{*4}	PDR19[R/W] B,H,W XXXXXXXX ^{*4}	
000014 _H to 000038 _H	—	—	—	—	Reserved
00003C _H	WDTCR0[R/W] B,H,W -0--0000	WDTCSR0[W] B,H,W 00000000	WDTCR1[R] B,H,W ---0110	WDTCSR1[W] B,H,W 00000000	Watchdog timer [S]
000040 _H	—	—	—	—	Reserved
000044 _H	DICR [R/W] B -----0	—	—	—	Delayed interrupt
000048 _H	TMRLRA4 [R/W] H XXXXXXXX XXXXXXXX		TMR4 [R] H XXXXXXXX XXXXXXXX		Reload timer 4
00004C _H	TMRLRB4 [R/W] H XXXXXXXX XXXXXXXX		TMCSR4 [R/W] B, H,W 00000000 0-000000		
000050 _H	TMRLRA5 [R/W] H XXXXXXXX XXXXXXXX		TMR5 [R] H XXXXXXXX XXXXXXXX		Reload timer 5
000054 _H	TMRLRB5 [R/W] H XXXXXXXX XXXXXXXX		TMCSR5 [R/W] B, H,W 00000000 0-000000		
000058 _H	TMRLRA6 [R/W] H XXXXXXXX XXXXXXXX		TMR6 [R] H XXXXXXXX XXXXXXXX		Reload timer 6
00005C _H	TMRLRB6 [R/W] H XXXXXXXX XXXXXXXX		TMCSR6 [R/W] B, H,W 00000000 0-000000		
000060 _H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		Reload timer 0
000064 _H	TMRLRB0 [R/W] H XXXXXXXX XXXXXXXX		TMCSR0 [R/W] B, H,W 00000000 0-000000		
000068 _H to 00007C _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000080 _H	BT0TMR[R] H 00000000 00000000		BT0TMCR[R/W]H -0000000 00000000		Base timer 0
000084 _H	—	BT0STC[R/W] B 0000-000	—	—	
000088 _H	BT0PCSR/BT0PRLL[R/W] H XXXXXXXX XXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF[R/W] H XXXXXXXX XXXXXXXX		Base timer 0
00008C _H	—	—	—	—	Reserved
000090 _H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W]H -0000000 00000000		Base timer 1
000094 _H	—	BT1STC[R/W] B 0000-000	—	—	
000098 _H	BT1PCSR/BT1PRLL[R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF[R/W] H 00000000 00000000		
00009C _H	BTSEL01[R/W] B ---0000	—	BTSSSR[W] B,H -----11		Base timer 0,1
0000A0 _H	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		
0000A4 _H	ADCS1 [R/W] B, H,W 0000000-	ADCS0 [R/W] B, H,W 000-----	ADCR1 [R] B, H,W -----XX	ADCR0 [R] B, H,W XXXXXXXX	A/D converter
0000A8 _H	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W --000000	ADECH [R/W] B, H,W --000000	
0000AC _H	—	EADERLL [R/W] B, H,W 00000000	EADCS [R] B, H,W --000000	—	
0000B0 _H	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000-0000	SSR0 [R/W] B,H,W 0-000011	ESCR0/(IBSR0) [R/W] B,H,W -0000000	Multi-UART0
0000B4 _H	RDR0/(TDR0)[R/W] B,H,W *1 -----0 00000000		BGR0 [R/W] H,W 00000000 00000000		*1: Byte access is permitted only for access to lower 8 bits
0000B8 _H	— / (ISMK0) [R/W] B,H,W ----- *2	— / (ISBA0) [R/W] B,H,W ----- *2	—	—	*2: Reserved because I ² C mode is not set immediately after reset.
0000BC _H	FCR10 [R/W] B,H,W ---00100	FCR00 [R/W] B,H,W -0000000	FBYTE20 [R/W] B,H,W 00000000	FBYTE10 [R/W] B,H,W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0000C0 _H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1 [R/W] B,H,W 000-0000	SSR1 [R/W] B,H,W 0-000011	ESCR1/(IBSR1) [R/W] B,H,W -0000000	Multi-UART1 *1: Byte access is permitted only for access to lower 8 bits *2: Reserved because I ² C mode is not set immediately after reset.
0000C4 _H	RDR1/(TDR1)[R/W] B,H,W *1 -----0 00000000		BGR1 [R/W] H,W 00000000 00000000		
0000C8 _H	— / (ISMK1) [R/W] B,H,W ----- *2	— / (ISBA1) [R/W] B,H,W ----- *2	—	—	
0000CC _H	FCR11 [R/W] B,H,W ---00100	FCR01 [R/W] B,H,W -0000000	FBYTE21 [R/W] B,H,W 00000000	FBYTE11 [R/W] B,H,W 00000000	
0000D0 _H	SCR2 [R/W] B, H, W 00000000	SMR2 [R/W] B, H, W 00000000	SSR2 [R/W] B, H, W 00001000	RDR2 /TDR2 [R/W] B, H, W 00000000	LIN-UART2
0000D4 _H	ESCR2 [R/W] B, H, W 00000X00	ECCR2 [R/W] B, H, W -0000-XX	BGR2 [R/W] B, H, W -0000000 00000000		
0000D8 _H	SCR3 [R/W] B, H, W 00000000	SMR3 [R/W] B, H, W 00000000	SSR3 [R/W] B, H, W 00001000	RDR3 /TDR3 [R/W] B, H, W 00000000	LIN-UART3
0000DC _H	ESCR3 [R/W] B, H, W 00000X00	ECCR3 [R/W] B, H, W -0000-XX	BGR3 [R/W] B, H, W -0000000 00000000		
0000E0 _H	SCR4 [R/W] B, H, W 00000000	SMR4 [R/W] B, H, W 00000000	SSR4 [R/W] B, H, W 00001000	RDR4 /TDR4 [R/W] B, H, W 00000000	LIN-UART4
0000E4 _H	ESCR4 [R/W] B, H, W 00000X00	ECCR4 [R/W] B, H, W -0000-XX	BGR4 [R/W] B, H, W -0000000 00000000		
0000E8 _H	SCR5 [R/W] B, H, W 00000000	SMR5 [R/W] B, H, W 00000000	SSR5 [R/W] B, H, W 00001000	RDR5 /TDR5 [R/W] B, H, W 00000000	LIN-UART5
0000EC _H	ESCR5 [R/W] B, H, W 00000X00	ECCR5 [R/W] B, H, W -0000-XX	BGR5 [R/W] B, H, W -0000000 00000000		
0000F0 _H	SCR6 [R/W] B, H, W 00000000	SMR6 [R/W] B, H, W 00000000	SSR6 [R/W] B, H, W 00001000	RDR6 /TDR6 [R/W] B, H, W 00000000	LIN-UART6
0000F4 _H	ESCR6 [R/W] B, H, W 00000X00	ECCR6 [R/W] B, H, W -0000-XX	BGR6 [R/W] B, H, W -0000000 00000000		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0000F8 _H	SCR7 [R/W] B, H, W 00000000	SMR7 [R/W] B, H, W 00000000	SSR7 [R/W] B, H, W 00001000	RDR7 /TDR7 [R/W] B, H, W 00000000	LIN-UART7
0000FC _H	ESCR7 [R/W] B, H, W 00000X00	ECCR7 [R/W] B, H, W -0000-XX	BGR7 [R/W] B, H, W -00000000 00000000		
000100 _H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104 _H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000		
000108 _H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload timer 2
00010C _H	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B, H,W 00000000 0-000000		
000110 _H	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114 _H	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B, H,W 00000000 0-000000		
000118 _H to 00011C _H	—	—	—	—	Reserved
000120 _H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				Output compare 6,7
000124 _H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
000128 _H	OCFS67 [R/W] B, H, W -----11	—	OCSH67[R/W] B, H, W --0--00	OCSL67[R/W] B, H, W 0000--00	
00012C _H	OCCP8 [R/W] W 00000000 00000000 00000000 00000000				Output compare 8,9
000130 _H	OCCP9 [R/W] W 00000000 00000000 00000000 00000000				
000134 _H	OCFS89 [R/W] B, H, W -----11	—	OCSH89[R/W] B, H, W --0--00	OCSL89[R/W] B, H, W 0000--00	
000138 _H	OCCP10 [R/W] W 00000000 00000000 00000000 00000000				Output compare 10,11
00013C _H	OCCP11 [R/W] W 00000000 00000000 00000000 00000000				
000140 _H	OCFS1011 [R/W] B, H, W -----11	—	OCSH1011[R/W] B, H, W --0--00	OCSL1011[R/W] B, H, W 0000--00	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000144 _H	GCN13 [R/W] H 00110010 00010000		—	GCN23 [R/W] B ----0000	PPG12, 13, 14, 15 control
000148 _H	GCN14 [R/W] H 00110010 00010000		—	GCN24 [R/W] B ----0000	PPG16, 17, 18, 19 control
00014C _H	GCN15 [R/W] H 00110010 00010000		—	GCN25 [R/W] B ----0000	PPG20, 21, 22, 23 control
000150 _H	PTMR11 [R] H,W 11111111 11111111		PCSR11 [W] H,W XXXXXXXX XXXXXXXX		PPG11
000154 _H	PDUT11 [W] H,W XXXXXXXX XXXXXXXX		PCN11 [R/W] B,H,W 0000000- 0000000-0		
000158 _H	PTMR12 [R] H,W 11111111 11111111		PCSR12 [W] H,W XXXXXXXX XXXXXXXX		PPG12
00015C _H	PDUT12 [W] H,W XXXXXXXX XXXXXXXX		PCN12 [R/W] B,H,W 0000000- 0000000-0		
000160 _H	PTMR13 [R] H,W 11111111 11111111		PCSR13 [W] H,W XXXXXXXX XXXXXXXX		PPG13
000164 _H	PDUT13 [W] H,W XXXXXXXX XXXXXXXX		PCN13 [R/W] B,H,W 0000000- 0000000-0		
000168 _H	PTMR14 [R] H,W 11111111 11111111		PCSR14 [W] H,W XXXXXXXX XXXXXXXX		PPG14
00016C _H	PDUT14 [W] H,W XXXXXXXX XXXXXXXX		PCN14 [R/W] B,H,W 0000000- 0000000-0		
000170 _H	PTMR15 [R] H,W 11111111 11111111		PCSR15 [W] H,W XXXXXXXX XXXXXXXX		PPG15
000174 _H	PDUT15 [W] H,W XXXXXXXX XXXXXXXX		PCN15 [R/W] B,H,W 0000000- 0000000-0		
000178 _H	PTMR16 [R] H,W 11111111 11111111		PCSR16 [W] H,W XXXXXXXX XXXXXXXX		PPG16
00017C _H	PDUT16 [W] H,W XXXXXXXX XXXXXXXX		PCN16 [R/W] B,H,W 0000000- 0000000-0		
000180 _H	PTMR17 [R] H,W 11111111 11111111		PCSR17 [W] H,W XXXXXXXX XXXXXXXX		PPG17
000184 _H	PDUT17 [W] H,W XXXXXXXX XXXXXXXX		PCN17 [R/W] B,H,W 0000000- 0000000-0		
000188 _H	PTMR18 [R] H,W 11111111 11111111		PCSR18 [W] H,W XXXXXXXX XXXXXXXX		PPG18
00018C _H	PDUT18 [W] H,W XXXXXXXX XXXXXXXX		PCN18 [R/W] B,H,W 0000000- 0000000-0		
000190 _H	PTMR19 [R] H,W 11111111 11111111		PCSR19 [W] H,W XXXXXXXX XXXXXXXX		PPG19
000194 _H	PDUT19 [W] H,W XXXXXXXX XXXXXXXX		PCN19 [R/W] B,H,W 0000000- 0000000-0		
000198 _H	PTMR20 [R] H,W 11111111 11111111		PCSR20 [W] H,W XXXXXXXX XXXXXXXX		PPG20
00019C _H	PDUT20 [W] H,W XXXXXXXX XXXXXXXX		PCN20 [R/W] B,H,W 0000000- 0000000-0		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0001A0 _H	PTMR21 [R] H,W 11111111 11111111		PCSR21 [W] H,W XXXXXXXX XXXXXXXX		PPG21
0001A4 _H	PDUT21 [W] H,W XXXXXXXX XXXXXXXX		PCN21 [R/W] B,H,W 0000000- 000000-0		
0001A8 _H	PTMR22 [R] H,W 11111111 11111111		PCSR22 [W] H,W XXXXXXXX XXXXXXXX		PPG22
0001AC _H	PDUT22 [W] H,W XXXXXXXX XXXXXXXX		PCN22 [R/W] B,H,W 0000000- 000000-0		
0001B0 _H	PTMR23 [R] H,W 11111111 11111111		PCSR23 [W] H,W XXXXXXXX XXXXXXXX		PPG23
0001B4 _H	PDUT23 [W] H,W XXXXXXXX XXXXXXXX		PCN23 [R/W] B,H,W 0000000- 000000-0		
0001B8 _H to 0001FC _H	—	—	—	—	Reserved
000200 _H	PWC20 [R/W] H,W -----XX XXXXXXXX		PWC10 [R/W] H,W -----XX XXXXXXXX		Stepping motor controller 0
000204 _H	—	PWC0 [R/W] B -00000--	PWS20 [R/W] B,H,W -0000000	PWS10 [R/W] B,H,W --000000	
000208 _H	PWC21 [R/W] H,W -----XX XXXXXXXX		PWC11 [R/W] H,W -----XX XXXXXXXX		Stepping motor controller 1
00020C _H	—	PWC1 [R/W] B -00000--	PWS21 [R/W] B,H,W -0000000	PWS11 [R/W] B,H,W --000000	
000210 _H	PWC22 [R/W] H,W -----XX XXXXXXXX		PWC12 [R/W] H,W -----XX XXXXXXXX		Stepping motor controller 2
000214 _H	—	PWC2 [R/W] B -00000--	PWS22 [R/W] B,H,W -0000000	PWS12 [R/W] B,H,W --000000	
000218 _H	PWC23 [R/W] H,W -----XX XXXXXXXX		PWC13 [R/W] H,W -----XX XXXXXXXX		Stepping motor controller3
00021C _H	—	PWC3 [R/W] B -00000--	PWS23 [R/W] B,H,W -0000000	PWS13 [R/W] B,H,W --000000	
000220 _H	PWC24 [R/W] H,W -----XX XXXXXXXX		PWC14 [R/W] H,W -----XX XXXXXXXX		Stepping motor controller 4
000224 _H	—	PWC4 [R/W] B -00000--	PWS24 [R/W] B,H,W -0000000	PWS14 [R/W] B,H,W --000000	
000228 _H	PWC25 [R/W] H,W -----XX XXXXXXXX		PWC15 [R/W] H,W -----XX XXXXXXXX		Stepping motor controller 5
00022C _H	—	PWC5 [R/W] B -00000--	PWS25 [R/W] B,H,W -0000000	PWS15 [R/W] B,H,W --000000	
000230 _H to 000238 _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
00023C _H	DACR0 [R/W] B,H,W -----0	DADR0 [R/W] B,H,W XXXXXXXX	DACR1 [R/W] B,H,W -----0	DADR1 [R/W] B,H,W XXXXXXXX	DA converter
000240 _H	CPCLR0 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 0
000244 _H	TCDT0 [R/W] W 00000000 00000000 00000000 00000000				
000248 _H	TCCSH0 [R/W]B,H,W 0----00	TCCSL0 [R/W]B,H,W -1-00000	—		
00024C _H	CPCLR1 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 1
000250 _H	TCDT1 [R/W] W 00000000 00000000 00000000 00000000				
000254 _H	TCCSH1 [R/W]B,H,W 0----00	TCCSL1 [R/W]B,H,W -1-00000	—		
000258 _H	—	—	—	—	Reserved
00025C _H	GCN10 [R/W] H 00110010 00010000		—	GCN20 [R/W] B ----0000	PPG0, 1, 2, 3 control
000260 _H	GCN11 [R/W] H 00110010 00010000		—	GCN21 [R/W] B ----0000	PPG4, 5, 6, 7 control
000264 _H	GCN12 [R/W] H 00110010 00010000		—	GCN22 [R/W] B ----0000	PPG8, 9, 10, 11 control
000268 _H	—	—	—	PPGDIV [R/W] B -----00	PPG0
00026C _H	PTMR0 [R] H,W 11111111 11111111		PCSR0 [W] H,W XXXXXXXX XXXXXXXX		
000270 _H	PDUT0 [W] H,W XXXXXXXX XXXXXXXX		PCN0 [R/W] B, H,W 0000000- 000000-0		
000274 _H	PTMR1 [R] H,W 11111111 11111111		PCSR1 [W] H,W XXXXXXXX XXXXXXXX		PPG1
000278 _H	PDUT1 [W] H,W XXXXXXXX XXXXXXXX		PCN1 [R/W] B,H,W 0000000- 000000-0		
00027C _H	PTMR2 [R] H,W 11111111 11111111		PCSR2 [W] H,W XXXXXXXX XXXXXXXX		PPG2
000280 _H	PDUT2 [W] H,W XXXXXXXX XXXXXXXX		PCN2 [R/W] B,H,W 0000000- 000000-0		
000284 _H	PTMR3 [R] H,W 11111111 11111111		PCSR3 [W] H,W XXXXXXXX XXXXXXXX		PPG3
000288 _H	PDUT3 [W] H,W XXXXXXXX XXXXXXXX		PCN3 [R/W] B,H,W 0000000- 000000-0		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
00028C _H	PTMR4 [R] H,W 11111111 11111111		PCSR4 [W] H,W XXXXXXXX XXXXXXXX		PPG4
000290 _H	PDUT4 [W] H,W XXXXXXXX XXXXXXXX		PCN4 [R/W] B,H,W 0000000- 000000-0		
000294 _H	PTMR5 [R] H,W 11111111 11111111		PCSR5 [W] H,W XXXXXXXX XXXXXXXX		PPG5
000298 _H	PDUT5 [W] H,W XXXXXXXX XXXXXXXX		PCN5 [R/W] B,H,W 0000000- 000000-0		
00029C _H	PTMR6 [R] H,W 11111111 11111111		PCSR6 [W] H,W XXXXXXXX XXXXXXXX		PPG6
0002A0 _H	PDUT6 [W] H,W XXXXXXXX XXXXXXXX		PCN6 [R/W] B,H,W 0000000- 000000-0		
0002A4 _H	PTMR7 [R] H,W 11111111 11111111		PCSR7 [W] H,W XXXXXXXX XXXXXXXX		PPG7
0002A8 _H	PDUT7 [W] H,W XXXXXXXX XXXXXXXX		PCN7 [R/W] B,H,W 0000000- 000000-0		
0002AC _H	PTMR8 [R] H,W 11111111 11111111		PCSR8 [W] H,W XXXXXXXX XXXXXXXX		PPG8
0002B0 _H	PDUT8 [W] H,W XXXXXXXX XXXXXXXX		PCN8 [R/W] B,H,W 0000000- 000000-0		
0002B4 _H	PTMR9 [R] H,W 11111111 11111111		PCSR9 [W] H,W XXXXXXXX XXXXXXXX		PPG9
0002B8 _H	PDUT9 [W] H,W XXXXXXXX XXXXXXXX		PCN9 [R/W] B,H,W 0000000- 000000-0		
0002BC _H	PTMR10 [R] H,W 11111111 11111111		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
0002C0 _H	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PCN10 [R/W] B,H,W 0000000- 000000-0		
0002C4 _H	IPCP0 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 0,1
0002C8 _H	IPCP1 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0002CC _H	ICFS01 [R/W] B, H, W -----00	—	LSYNS0 [R/W] B,H,W --000000	ICS01 [R/W] B, H, W 00000000	
0002D0 _H	IPCP2 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 2,3
0002D4 _H	IPCP3 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0002D8 _H	ICFS23 [R/W] B, H, W -----00	—	—	ICS23 [R/W] B, H, W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0002DC _H	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 4,5
0002E0 _H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0002E4 _H	ICFS45 [R/W] B, H, W -----00	—	—	ICS45 [R/W] B, H, W 00000000	
0002E8 _H	OCCP0 [R/W] W 00000000 00000000 00000000 00000000				Output compare 0,1
0002EC _H	OCCP1 [R/W] W 00000000 00000000 00000000 00000000				
0002F0 _H	OCFS01 [R/W] B, H, W -----11	—	OCSH01[R/W] B, H, W --0--00	OCSL01[R/W] B, H, W 0000--00	
0002F4 _H	OCCP2 [R/W] W 00000000 00000000 00000000 00000000				Output compare 2,3
0002F8 _H	OCCP3 [R/W] W 00000000 00000000 00000000 00000000				
0002FC _H	OCFS23 [R/W] B, H, W -----11	—	OCSH23[R/W] B, H, W --0--00	OCSL23[R/W] B, H, W 0000--00	
000300 _H to 00030C _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000310 _H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314 _H	—	—	—	—	
000318 _H	—				
00031C _H	—	—	—		
000320 _H	DPVAR [R] W XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX				
000324 _H	—	—	DPVSR [R/W] H ----- 00000--0		
000328 _H	DEAR [R] W XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX				
00032C _H	—	—	DESR [R/W] H ----- 00000--0		
000330 _H	PABR0 [R/W] W XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000				
000334 _H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338 _H	PABR1 [R/W] W XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000				
00033C _H	—	—	PACR1 [R/W] H 000000-0 00000--0		
000340 _H	PABR2 [R/W] W XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000				
000344 _H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348 _H	PABR3 [R/W] W XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000				
00034C _H	—	—	PACR3 [R/W] H 000000-0 00000--0		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000350 _H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only the CPU can access this area)
000354 _H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358 _H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00035C _H	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360 _H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364 _H	—	—	PACR6 [R/W] H 000000-0 00000--0		
000368 _H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00036C _H	—	—	PACR7 [R/W] H 000000-0 00000--0		
000370 _H	PABR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only product supporting MPU 12 channels or 16 channels) (Only the CPU can access this area)
000374 _H	—	—	PACR8 [R/W] H 000000-0 00000--0		
000378 _H	PABR9[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00037C _H	—	—	PACR9 [R/W] H 000000-0 00000--0		
000380 _H	PABR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000384 _H	—	—	PACR10 [R/W] H 000000-0 00000--0		
000388 _H	PABR11 [R/W] ,W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00038C _H	—	—	PACR11 [R/W] H 000000-0 00000--0		
000390 _H	PABR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000394 _H	—	—	PACR12 [R/W] H 000000-0 00000--0		
000398 _H	PABR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00039C _H	—	—	PACR13 [R/W] H 000000-0 00000--0		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0003A0 _H	PABR14 [R/W]W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only product supporting MPU 16 channels) (Only the CPU can access this area)
0003A4 _H	—	—	PACR14 [R/W] H 000000-0 00000--0		
0003A8 _H	PABR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
0003AC _H	—	—	PACR15 [R/W] H 000000-0 00000--0		
0003B0 _H to 0003FC _H	—	—	—	—	Reserved [S]
000400 _H	ICSEL0[R/W] B, H, W -----000	ICSEL1[R/W] B, H, W -----000	ICSEL2[R/W] B, H, W -----0	ICSEL3[R/W] B, H, W -----0	Generation and clear of DMA transfer request
000404 _H	ICSEL4[R/W] B, H, W -----0	ICSEL5[R/W] B, H, W -----0	ICSEL6[R/W] B, H, W -----000	ICSEL7[R/W] B, H, W -----000	
000408 _H	ICSEL8[R/W] B, H, W -----00	ICSEL9[R/W] B, H, W -----00	ICSEL10 [R/W]B, H, W -----00	ICSEL11[R/W] B, H, W -----00	
00040C _H	ICSEL12[R/W] B, H, W -----00	ICSEL13[R/W] B, H, W -----0	ICSEL14 [R/W]B, H, W -----0	ICSEL15[R/W] B, H, W -----0	
000410 _H	ICSEL16[R/W] B, H, W -----0	ICSEL17[R/W] B, H, W -----0	ICSEL18 [R/W]B, H, W -----0	ICSEL19[R/W] B, H, W -----000	
000414 _H	ICSEL20[R/W] B, H, W -----000	ICSEL21[R/W] B, H, W -----00	ICSEL22 [R/W]B, H, W -----00	—	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000418 _H	IRPR0H[R] B, H, W 00-----	IRPR0L[R] B, H, W 00-----	IRPR1H[R] B, H, W 00-----	IRPR1L[R] B, H, W 00-----	Interrupt request batch read register
00041C _H	IRPR2H[R] B, H, W 00-----	IRPR2L[R] B, H, W 00-----	IRPR3H[R] B, H, W 000000--	IRPR3L[R] B, H, W 000000--	
000420 _H	IRPR4H[R] B, H, W 0000----	IRPR4L[R] B, H, W 0000----	IRPR5H[R] B, H, W 0000----	IRPR5L[R] B, H, W 000-----	
000424 _H	IRPR6H[R] B, H, W --000---	IRPR6L[R] B, H, W 000000---	IRPR7H[R] B, H, W -0000---	IRPR7L[R] B, H, W -----00	
000428 _H	IRPR8H[R] B, H, W 000-----	IRPR8L[R] B, H, W 000-----	IRPR9H[R] B, H, W 00-----	IRPR9L[R] B, H, W 00-----	
00042C _H	IRPR10H[R] B, H, W 00-----	IRPR10L[R] B, H, W 00-----	IRPR11H[R] B, H, W 00-----	IRPR11L[R] B, H, W 00-----	
000430 _H	IRPR12H[R] B, H, W 000000--	IRPR12L[R] B, H, W 000000--	IRPR13H[R] B, H, W 000-----	IRPR13L[R] B, H, W 000000--	
000434 _H	IRPR14H[R] B, H, W 00000000	IRPR14L[R] B, H, W 00000000	IRPR15H[R] B, H, W 000-----	—	Interrupt request batch read register
000438 _H to 00043C _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000440 _H	ICR00 [R/W] B, H, W ---11111	ICR01 [R/W] B, H, W ---11111	ICR02 [R/W] B, H, W ---11111	ICR03 [R/W] B, H, W ---11111	Interrupt controller [S]
000444 _H	ICR04 [R/W] B, H, W ---11111	ICR05 [R/W] B, H, W ---11111	ICR06 [R/W] B, H, W ---11111	ICR07 [R/W] B, H, W ---11111	
000448 _H	ICR08 [R/W] B, H, W ---11111	ICR09 [R/W] B, H, W ---11111	ICR10 [R/W] B, H, W ---11111	ICR11 [R/W] B, H, W ---11111	
00044C _H	ICR12 [R/W] B, H, W ---11111	ICR13 [R/W] B, H, W ---11111	ICR14 [R/W] B, H, W ---11111	ICR15 [R/W] B, H, W ---11111	
000450 _H	ICR16 [R/W] B, H, W ---11111	ICR17 [R/W] B, H, W ---11111	ICR18 [R/W] B, H, W ---11111	ICR19 [R/W] B, H, W ---11111	
000454 _H	ICR20 [R/W] B, H, W ---11111	ICR21 [R/W] B, H, W ---11111	ICR22 [R/W] B, H, W ---11111	ICR23 [R/W] B, H, W ---11111	
000458 _H	ICR24 [R/W] B, H, W ---11111	ICR25 [R/W] B, H, W ---11111	ICR26 [R/W] B, H, W ---11111	ICR27 [R/W] B, H, W ---11111	
00045C _H	ICR28 [R/W] B, H, W ---11111	ICR29 [R/W] B, H, W ---11111	ICR30 [R/W] B, H, W ---11111	ICR31 [R/W] B, H, W ---11111	
000460 _H	ICR32 [R/W] B, H, W ---11111	ICR33 [R/W] B, H, W ---11111	ICR34 [R/W] B, H, W ---11111	ICR35 [R/W] B, H, W ---11111	
000464 _H	ICR36 [R/W] B, H, W ---11111	ICR37 [R/W] B, H, W ---11111	ICR38 [R/W] B, H, W ---11111	ICR39 [R/W] B, H, W ---11111	
000468 _H	ICR40 [R/W] B, H, W ---11111	ICR41 [R/W] B, H, W ---11111	ICR42 [R/W] B, H, W ---11111	ICR43 [R/W] B, H, W ---11111	
00046C _H	ICR44 [R/W] B, H, W ---11111	ICR45 [R/W] B, H, W ---11111	ICR46 [R/W] B, H, W ---11111	ICR47 [R/W] B, H, W ---11111	
000470 _H to 00047C _H	—	—	—	—	
000480 _H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111----0	STBCR [R/W] B,H,W * 000---11	—	Reset control [S] Power consumption control [S] *: Writing to STBCR by DMA is not permitted
000484 _H	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000488 _H	DIVR0 [R/W] B,H,W 000-----	DIVR1 [R/W] B,H,W 0001----	DIVR2 [R/W] B,H,W 0011----	—	Clock control [S]
00048C _H	—	—	—	—	Reserved [S]
000490 _H	IORR0[R/W] B, H, W -0000000	IORR1[R/W] B, H, W -0000000	IORR2[R/W] B, H, W -0000000	IORR3[R/W] B, H, W -0000000	DMA transfer request from a peripheral [S]
000494 _H	IORR4[R/W] B, H, W -0000000	IORR5[R/W] B, H, W -0000000	IORR6[R/W] B, H, W -0000000	IORR7[R/W] B, H, W -0000000	
000498 _H	IORR8[R/W] B, H, W -0000000	IORR9[R/W] B, H, W -0000000	IORR10[R/W] B, H, W -0000000	IORR11[R/W] B, H, W -0000000	
00049C _H	IORR12[R/W] B, H, W -0000000	IORR13[R/W] B, H, W -0000000	IORR14[R/W] B, H, W -0000000	IORR15[R/W] B, H, W -0000000	
0004A0 _H	—	—	—	—	Reserved
0004A4 _H	CANPRE [R/W] B,H,W ----0000	—	—	—	CAN prescaler
0004A8 _H to 0004B4 _H	—	—	—	—	Reserved
0004B8 _H	CUCR0 [R/W] B,H,W ----- --0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration (Calibration)
0004BC _H	CUTR0 [R] B,H,W ----- 00000000 00000000 00000000				
0004C0 _H	—	—	—	—	
0004C4 _H	CUCR1 [R/W] B,H,W ----- --0--00		CUTD1[R/W] B,H,W 11000011 01010000		
0004C8 _H	CUTR1 [R] B,H,W ----- 00000000 00000000 00000000				
0004CC _H	CRTR [R/W] B,H,W 01111111	—	—	—	
0004D0 _H to 0004DC _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0004E0 _H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8 [R/W] B,H,W 000-0000	SSR8 [R/W] B,H,W 0-000011	ESCR8/(IBSR8) [R/W] B,H,W -0000000	Multi-UART8 *1: Byte access is permitted only for access to lower 8 bits
0004E4 _H	RDR8/(TDR8)[R/W] B,H,W *1 -----0 00000000		BGR8 [R/W] H,W 00000000 00000000		
0004E8 _H	—	—	—	—	
0004EC _H	FCR18 [R/W] B,H,W ---00100	FCR08 [R/W] B,H,W -0000000	FBYTE28 [R/W] B,H,W 00000000	FBYTE18 [R/W] B,H,W 00000000	
0004F0 _H	SCR9/(IBCR9) [R/W] B,H,W 0-00000	SMR9 [R/W] B,H,W 000-0000	SSR9 [R/W] B,H,W 0-000011	ESCR9/(IBSR9) [R/W] B,H,W -0000000	Multi-UART9 *1: Byte access is permitted only for access to lower 8 bits
0004F4 _H	RDR9/(TDR9)[R/W] B,H,W *1 -----0 00000000		BGR9 [R/W] H,W 00000000 00000000		
0004F8 _H	—	—	—	—	
0004FC _H	FCR19 [R/W] B,H,W ---00100	FCR09 [R/W] B,H,W -0000000	FBYTE29 [R/W] B,H,W 00000000	FBYTE19 [R/W] B,H,W 00000000	
000500 _H to 00050C _H	—	—	—	—	Reserved
000510 _H	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock control [S]
000514 _H	PLLCR [R/W] B,H,W ----- 11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00-----	
000518 _H	—	—	CPUAR [R/W] B,H,W 0---XXX	—	Reset [S]
00051C _H	—	—	—	—	Reserved [S]
000520 _H	CCPSELR [R/W] B,H,W -----0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock control 2
000524 _H	—	CCPLLFB [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528 _H	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1[R/W]H,W 000-----		
00052C _H	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000530 _H	CCRTSELR [R/W] B,H,W 0-----0	—	CCPMUCR0 [R/W] B,H,W 0-----0	CCPMUCR1 [R/W] B,H,W 0--00000	Clock control 2
000534 _H	—	—	—	—	
000538 _H	—	—	—	—	
00053C _H	—	—	—	—	
000540 _H to 00054C _H	—	—	—	—	Reserved
000550 _H	EIRR0[R/W] B,H,W XXXXXXXX	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt (INT0 to INT7)
000554 _H	EIRR1[R/W] B,H,W XXXXXXXX	ENIR1[R/W] B,H,W 00000000	ELVR1[R/W] B,H,W 00000000 00000000		External interrupt (INT8 to INT15)
000558 _H	—	—	—	—	Reserved
00055C _H	—	—	WTDR[R/W] H 00000000 00000000		Real-time clock
000560 _H	—	WTCRH [R/W] B -----00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H ----00-0	
000564 _H	—	WTRH [R/W] B --XXXXXX	WTRM [R/W] B XXXXXXXX	WTRL [R/W] B XXXXXXXX	
000568 _H	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—	
00056C _H	—	CSVCR[R/W]B -001110- -001010-*3	—	—	Clock supervisor
000570 _H to 00057C _H	—	—	—	—	Reserved
000580 _H	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator control
000584 _H	LVD5R [R/W] B,H,W -----1	LVD5F [R/W] B,H,W 0-100--1	LVD [R/W] B,H,W 01000--0	—	Low-voltage detection
000588 _H to 00058C _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000590 _H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR [R/W] B,H,W 0-00----	PWRTMCTL [R/W] B,H,W -----011	—	PMU
000594 _H	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	—	
000598 _H	—	—	—	—	
00059C _H to 0005A4 _H	—	—	—	—	Reserved
0005A8 _H	LCDCMR [R/W] B,H,W 0-----	LCRS [R/W] B,H,W 00000000	LCR0 [R/W] B,H,W 00010000	LCR1 [R/W] B,H,W -----	LCD controller
0005AC _H	VRAM0[R/W] B,H,W 00000000	VRAM1[R/W] B,H,W 00000000	VRAM2[R/W] B,H,W 00000000	VRAM3[R/W] B,H,W 00000000	
0005B0 _H	VRAM4[R/W] B,H,W 00000000	VRAM5[R/W] B,H,W 00000000	VRAM6[R/W] B,H,W 00000000	VRAM7[R/W] B,H,W 00000000	
0005B4 _H	VRAM8[R/W] B,H,W 00000000	VRAM9[R/W] B,H,W 00000000	VRAM10[R/W] B,H,W 00000000	VRAM11[R/W] B,H,W 00000000	
0005B8 _H	VRAM12[R/W] B,H,W 00000000	VRAM13[R/W] B,H,W 00000000	VRAM14[R/W] B,H,W 00000000	VRAM15[R/W] B,H,W 00000000	
0005BC _H	LDR0[R/W] B,H,W -----0	LDR1[R/W] B,H,W 00000000	—	—	
0005C0 _H to 0005FC _H	—	—	—	—	
000600 _H	ASR0 [R/W] W 00000000 00000000 ----- 1111-001				External bus Interface [S]
000604 _H	ASR1 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0				
000608 _H	ASR2 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0				
00060C _H	ASR3 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0				
000610 _H to 00063C _H	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000640 _H	ACR0 [R/W] W ----- 01--00--				External bus Interface [S]
000644 _H	ACR1 [R/W] W ----- XX--XX--				
000648 _H	ACR2 [R/W] W ----- XX--XX--				
00064C _H	ACR3 [R/W] W ----- XX--XX--				
000650 _H to 00067C _H	—	—	—	—	Reserved [S]
000680 _H	AWR0 [R/W] W ----1111 00000000 11110000 00000-0-				External bus Interface [S]
000684 _H	AWR1 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000688 _H	AWR2 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
00068C _H	AWR3 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690 _H to 00070C _H	—	—	—	—	Reserved (to 0006FF _H [S])
000710 _H	BPCCR[A/R/W] B 00000000	BPCCR[B/R/W] B 00000000	BPCCR[C/R/W] B 00000000	—	Bus performance counter
000714 _H	BPCTRA [R/W] W 00000000 00000000 00000000 00000000				
000718 _H	BPCTRB [R/W] W 00000000 00000000 00000000 00000000				
00071C _H	BPCTRC [R/W] W 00000000 00000000 00000000 00000000				
000720 _H to 0007F8 _H	—	—	—	—	Reserved
0007FC _H	BMODR[R] B, H, W XXXXXXXX	—	—	—	Operation mode
000800 _H to 00083C _H	—	—	—	—	Reserved [S]
000840 _H	FCTLR[R/W] H -0--1000 0-0----		—	FSTR[R/W] B -----001	Flash memory register [S]
000844 _H	—	—	—	—	Reserved [S]
000848 _H	—	—	—	—	Reserved [S]
00084C _H	—	—	—	—	
000850 _H	—	—	—	—	
000854 _H	—	—	—	—	
000858 _H	—	—	WREN[R/W] H 00000000 00000000		Wild register [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
00085C _H	—	—	—	—	Reserved [S]
000860 _H	—	—	—	—	
000864 _H	—	—	—	—	
000868 _H	—	—	—	—	
00086C _H	—	—	—	—	
000870 _H	—	—	—	—	
000874 _H	—	—	—	—	
000878 _H	—	—	—	—	
00087C _H	—	—	—	—	Reserved [S]
000880 _H	WRAR00 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884 _H	WRDR00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888 _H	WRAR01 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
00088C _H	WRDR01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890 _H	WRAR02 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
000894 _H	WRDR02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898 _H	WRAR03 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
00089C _H	WRDR03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008A0 _H	WRAR04 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008A4 _H	WRDR04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008A8 _H	WRAR05 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008AC _H	WRDR05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B0 _H	WRAR06 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008B4 _H	WRDR06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B8 _H	WRAR07 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008BC _H	WRDR07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C0 _H	WRAR08 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008C4 _H	WRDR08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0008C8 _H	WRAR09 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
0008CC _H	WRDR09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D0 _H	WRAR10 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008D4 _H	WRDR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D8 _H	WRAR11 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008DC _H	WRDR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E0 _H	WRAR12 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008E4 _H	WRDR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E8 _H	WRAR13 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008EC _H	WRDR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F0 _H	WRAR14 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008F4 _H	WRDR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F8 _H	WRAR15 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008FC _H	WRDR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900 _H to 000BF8 _H	—	—	—	—	
000BFC _H	—	—	UER [W] B,H,W ----- --X		OCDU
000C00 _H	DCCR0[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
000C04 _H	DCSR0[R/W] H 0----- -----000		DTCR0[R/W] H 00000000 00000000		
000C08 _H	DSAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C0C _H	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C10 _H	DCCR1 [R/W] W 0----000 --00--00 00000000 0-000000				
000C14 _H	DCSR1 [R/W] H 0----- -----000		DTCR1 [R/W] H 00000000 00000000		
000C18 _H	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C1C _H	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000C20 _H	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
000C24 _H	DCSR2 [R/W] H 0-----000		DTCR2 [R/W] H 00000000 00000000		
000C28 _H	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C2C _H	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C30 _H	DCCR3[R/W] W 0----000 --00--00 00000000 0-000000				
000C34 _H	DCSR3 [R/W] H 0-----000		DTCR3 [R/W] H 00000000 00000000		
000C38 _H	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C3C _H	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C40 _H	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				
000C44 _H	DCSR4 [R/W] H 0-----000		DTCR4 [R/W] H 00000000 00000000		
000C48 _H	DSAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C4C _H	DDAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C50 _H	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				
000C54 _H	DCSR5 [R/W] H 0-----000		DTCR5 [R/W] H 00000000 00000000		
000C58 _H	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C5C _H	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C60 _H	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				
000C64 _H	DCSR6 [R/W] H 0-----000		DTCR6 [R/W] H 00000000 00000000		
000C68 _H	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C6C _H	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000C70 _H	DCCR7 [R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
000C74 _H	DCSR7 [R/W] H 0-----000		DTCR7 [R/W] H 00000000 00000000		
000C78 _H	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C7C _H	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C80 _H	DCCR8 [R/W] W 0----000 --00--00 00000000 0-000000				
000C84 _H	DCSR8 [R/W] H 0-----000		DTCR8 [R/W] H 00000000 00000000		
000C88 _H	DSAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C8C _H	DDAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C90 _H	DCCR9 [R/W] W 0----000 --00--00 00000000 0-000000				
000C94 _H	DCSR9 [R/W] H 0-----000		DTCR9 [R/W] H 00000000 00000000		
000C98 _H	DSAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C9C _H	DDAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CA0 _H	DCCR10 [R/W] W 0----000 --00--00 00000000 0-000000				
000CA4 _H	DCSR10[R/W] H 0-----000		DTCR10[R/W] H 00000000 00000000		
000CA8 _H	DSAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CAC _H	DDAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CB0 _H	DCCR11[R/W] W 0----000 --00--00 00000000 0-000000				
000CB4 _H	DCSR11 [R/W] H 0-----000		DTCR11 [R/W] H 00000000 00000000		
000CB8 _H	DSAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CBC _H	DDAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000CC0 _H	DCCR12 [R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
000CC4 _H	DCSR12 [R/W] H 0----- 000		DTCR12 [R/W] H 00000000 00000000		
000CC8 _H	DSAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CC _H	DDAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CD0 _H	DCCR13 [R/W] W 0----000 --00--00 00000000 0-000000				
000CD4 _H	DCSR13[R/W] H 0----- 000		DTCR13[R/W] H 00000000 00000000		
000CD8 _H	DSAR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CDC _H	DDAR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CE0 _H	DCCR14[R/W] W 0----000 --00--00 00000000 0-000000				
000CE4 _H	DCSR14[R/W] H 0----- 000		DTCR14[R/W] H 00000000 00000000		
000CE8 _H	DSAR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CE _H	DDAR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CF0 _H	DCCR15[R/W] W 0----000 --00--00 00000000 0-000000				
000CF4 _H	DCSR15[R/W] H 0----- 000		DTCR15[R/W] H 00000000 00000000		
000CF8 _H	DSAR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CF _H	DDAR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000D00 _H to 000DF0 _H	—	—	—	—	Reserved [S]
000DF4 _H	—	—	DNMIR[R/W] B 0-----0	DILVR[R/W] B ---11111	DMA controller [S]
000DF8 _H	DMACR[R/W] W 0----- 0-----				
000DF _H	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000E00 _H	DDR00[R/W] B,H,W 00000000	DDR01[R/W] B,H,W 00000000	DDR02[R/W] B,H,W 00000000	DDR03[R/W] B,H,W 00000000	Data direction Register *4:CY91F578/9 only
000E04 _H	DDR04[R/W] B,H,W 00000000	DDR05[R/W] B,H,W -00000000	DDR06[R/W] B,H,W 00000000	DDR07[R/W] B,H,W 00000000	
000E08 _H	DDR08[R/W] B,H,W 00000000	DDR09[R/W] B,H,W 00000000	DDR10[R/W] B,H,W 00000000	DDR11[R/W] B,H,W 00000000	
000E0C _H	DDR12[R/W] B,H,W 00000000	DDR13[R/W] B,H,W 00-000000	DDR14[R/W] B,H,W 00000000 ^{*4}	DDR15[R/W] B,H,W 00000000 ^{*4}	
000E10 _H	DDR16[R/W] B,H,W 00000000 ^{*4}	DDR17[R/W] B,H,W 00000000 ^{*4}	DDR18[R/W] B,H,W 00000000 ^{*4}	DDR19[R/W] B,H,W 00000000 ^{*4}	
000E14 _H to 000E1C _H	—	—	—	—	Reserved
000E20 _H	PFR00[R/W] B,H,W 00000000	PFR01[R/W] B,H,W 00000000	PFR02[R/W] B,H,W 00000000	PFR03[R/W] B,H,W 10000000	Port function register *4:CY91F578/9 only
000E24 _H	PFR04[R/W] B,H,W 11111111	PFR05[R/W] B,H,W 11111111	PFR06[R/W] B,H,W 00000000	PFR07[R/W] B,H,W 00000000	
000E28 _H	PFR08[R/W] B,H,W 00000000	PFR09[R/W] B,H,W 0-00000000	PFR10[R/W] B,H,W 00000000	PFR11[R/W] B,H,W 00000000	
000E2C _H	PFR12[R/W] B,H,W 00000000	PFR13[R/W] B,H,W 00-000000	PFR14[R/W] B,H,W 00000000 ^{*4}	PFR15[R/W] B,H,W 00000000 ^{*4}	
000E30 _H	PFR16[R/W] B,H,W 00000000 ^{*4}	PFR17[R/W] B,H,W 00000000 ^{*4}	PFR18[R/W] B,H,W 00000000 ^{*4}	PFR19[R/W] B,H,W 00000000 ^{*4}	
000E34 _H to 000E3C _H	—	—	—	—	Reserved
000E40 _H	PDDR00[R] B,H,W XXXXXXXXXX	PDDR01[R] B,H,W XXXXXXXXXX	PDDR02[R] B,H,W XXXXXXXXXX	PDDR03[R] B,H,W XXXXXXXXXX	Input data direct read register *4:CY91F578/9 only
000E44 _H	PDDR04[R] B,H,W XXXXXXXXXX	PDDR05[R] B,H,W XXXXXXXXXX	PDDR06[R] B,H,W XXXXXXXXXX	PDDR07[R] B,H,W XXXXXXXXXX	
000E48 _H	PDDR08[R] B,H,W XXXXXXXXXX	PDDR09[R] B,H,W XXXXXXXXXX	PDDR10[R] B,H,W XXXXXXXXXX	PDDR11[R] B,H,W XXXXXXXXXX	
000E4C _H	PDDR12[R] B,H,W XXXXXXXXXX	PDDR13[R] B,H,W XX-XXXXXX	PDDR14[R] B,H,W XXXXXXXXXX ^{*4}	PDDR15[R] B,H,W XXXXXXXXXX ^{*4}	
000E50 _H	PDDR16[R] B,H,W XXXXXXXXXX ^{*4}	PDDR17[R] B,H,W XXXXXXXXXX ^{*4}	PDDR18[R] B,H,W XXXXXXXXXX ^{*4}	PDDR19[R] B,H,W XXXXXXXXXX ^{*4}	
000E54 _H to 000E5C _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000E60 _H	EPFR00[R/W] B,H,W 00000000	EPFR01[R/W] B,H,W 00000000	EPFR02[R/W] B,H,W ---00000	EPFR03[R/W] B,H,W ---00000	Extended port function register
000E64 _H	EPFR04[R/W] B,H,W ---00000	EPFR05[R/W] B,H,W ---00000	EPFR06[R/W] B,H,W ---00000	EPFR07[R/W] B,H,W ---00000	
000E68 _H	EPFR08[R/W] B,H,W ---00000	EPFR09[R/W] B,H,W ---00000	EPFR10[R/W] B,H,W -0000000	EPFR11[R/W] B,H,W --000000	
000E6C _H	EPFR12[R/W] B,H,W --000000	EPFR13[R/W] B,H,W --000000	EPFR14[R/W] B,H,W --000000	EPFR15[R/W] B,H,W -0000000	
000E70 _H	EPFR16[R/W] B,H,W 00000000	EPFR17[R/W] B,H,W 00000000	EPFR18[R/W] B,H,W 10000000	EPFR19[R/W] B,H,W 11111111	
000E74 _H	EPFR20[R/W] B,H,W 11111111	EPFR21[R/W] B,H,W 00000000	EPFR22[R/W] B,H,W 00000000	EPFR23[R/W] B,H,W 00000000	
000E78 _H	EPFR24[R/W] B,H,W -----000	EPFR25[R/W] B,H,W -----000	EPFR26[R/W] B,H,W ----0000	EPFR27[R/W] B,H,W ---00000	
000E7C _H	EPFR28[R/W] B,H,W ----0000	EPFR29[R/W] B,H,W 00000000	EPFR30[R/W] B,H,W 00000000	EPFR31[R/W] B,H,W 00000000	
000E80 _H	EPFR32[R/W] B,H,W 00000000	EPFR33[R/W] B,H,W ---00000	EPFR34[R/W] B,H,W --00000	EPFR35[R/W] B,H,W ---00000	
000E84 _H	EPFR36[R/W] B,H,W ---00000	EPFR37[R/W] B,H,W 00000000	EPFR38[R/W] B,H,W --00000	EPFR39[R/W] B,H,W 00000000	
000E88 _H	EPFR40[R/W] B,H,W --000000	EPFR41[R/W] B,H,W -----000	EPFR42[R/W] B,H,W -----00	EPFR43[R/W] B,H,W 00000000	
000E8C _H	EPFR44[R/W] B,H,W 00000000	EPFR45[R/W] B,H,W 00000000	EPFR46[R/W] B,H,W --000000	EPFR47[R/W] B,H,W -----0	
000E90 _H	—	—	—	—	
000E94 _H	EPFR52[R/W] B,H,W -----0	EPFR53[R/W] B,H,W ---00000	EPFR54[R/W] B,H,W ----0000	—	
000E98 _H to 000E9C _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000EA0 _H	PPCR00[R/W] B,H,W 11111111	PPCR01[R/W] B,H,W 11111111	PPCR02[R/W] B,H,W 11111111	PPCR03[R/W] B,H,W 11111111	Port pull-up/down control register *4:CY91F578/9 only
000EA4 _H	PPCR04[R/W] B,H,W 11111111	PPCR05[R/W] B,H,W 11111111	PPCR06[R/W] B,H,W 11111111	PPCR07[R/W] B,H,W 11111111	
000EA8 _H	PPCR08[R/W] B,H,W 11111111	PPCR09[R/W] B,H,W 11111111	PPCR10[R/W] B,H,W 11111111	PPCR11[R/W] B,H,W 11111111	
000EAC _H	PPCR12[R/W] B,H,W 11111111	PPCR13[R/W] B,H,W 11-111111	PPCR14[R/W] B,H,W 11111111 ^{*4}	PPCR15[R/W] B,H,W 11-111111 ^{*4}	
000EB0 _H	PPCR16[R/W] B,H,W 11111111 ^{*4}	PPCR17[R/W] B,H,W 11111111 ^{*4}	PPCR18[R/W] B,H,W 11111111 ^{*4}	PPCR19[R/W] B,H,W 11-111111 ^{*4}	
000EBC _H	—	—	—	—	Reserved
000EC0 _H	PPER00[R/W] B,H,W 00000000	PPER01[R/W] B,H,W 00000000	PPER02[R/W] B,H,W 00000000	PPER03[R/W] B,H,W 00000000	Port pull-up/down enable register *4:CY91F578/9 only
000EC4 _H	PPER04[R/W] B,H,W 00000000	PPER05[R/W] B,H,W 00000000	PPER06[R/W] B,H,W 00000000	PPER07[R/W] B,H,W 00000000	
000EC8 _H	PPER08[R/W] B,H,W 00000000	PPER09[R/W] B,H,W 00000000	PPER10[R/W] B,H,W 00000000	PPER11[R/W] B,H,W 00000000	
000ECC _H	PPER12[R/W] B,H,W 00000000	PPER13[R/W] B,H,W 00-000000	PPER14[R/W] B,H,W 00000000 ^{*4}	PPER15[R/W] B,H,W 00000000 ^{*4}	
000ED0 _H	PPER16[R/W] B,H,W 00000000 ^{*4}	PPER17[R/W] B,H,W 00000000 ^{*4}	PPER18[R/W] B,H,W 00000000 ^{*4}	PPER19[R/W] B,H,W 00000000 ^{*4}	Reserved
000EDC _H	—	—	—	—	
000EE0 _H	PILR00[R/W] B,H,W 11111111	PILR01[R/W] B,H,W 11111111	PILR02[R/W] B,H,W 11111111	PILR03[R/W] B,H,W 11111111	Port input level selection register *4:CY91F578/9 only
000EE4 _H	PILR04[R/W] B,H,W 11111111	PILR05[R/W] B,H,W 11111111	PILR06[R/W] B,H,W 11111111	PILR07[R/W] B,H,W 11111111	
000EE8 _H	PILR08[R/W] B,H,W 11111111	PILR09[R/W] B,H,W 11111111	PILR10[R/W] B,H,W 11111111	PILR11[R/W] B,H,W 11111111	
000EEC _H	PILR12[R/W] B,H,W 11111111	PILR13[R/W] B,H,W 11-111111	PILR14[R/W] B,H,W 11111111 ^{*4}	PILR15[R/W] B,H,W 11111111 ^{*4}	
000EF0 _H	PILR16[R/W] B,H,W 11111111 ^{*4}	PILR17[R/W] B,H,W 11111111 ^{*4}	PILR18[R/W] B,H,W 11111111 ^{*4}	PILR19[R/W] B,H,W 11111111 ^{*4}	
000EFC _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000F00 _H	EPILR00[R/W] B,H,W 00000000	EPILR01[R/W] B,H,W 00000000	EPILR02[R/W] B,H,W 00000000	EPILR03[R/W] B,H,W 00000000	Extended Port input level selection register *4:CY91F578/9 only
000F04 _H	EPILR04[R/W] B,H,W 00000000	EPILR05[R/W] B,H,W 00000000	EPILR06[R/W] B,H,W 00000000	EPILR07[R/W] B,H,W 00000000	
000F08 _H	EPILR08[R/W] B,H,W 00000000	EPILR09[R/W] B,H,W 00000000	EPILR10[R/W] B,H,W 00000000	EPILR11[R/W] B,H,W 00000000	
000F0C _H	EPILR12[R/W] B,H,W 00000000	EPILR13[R/W] B,H,W 00-000000	EPILR14[R/W] B,H,W 00000000* ⁴	EPILR15[R/W] B,H,W 00000000* ⁴	
000F10 _H	EPILR16[R/W] B,H,W 00000000* ⁴	EPILR17[R/W] B,H,W 00000000* ⁴	EPILR18[R/W] B,H,W 00000000* ⁴	EPILR19[R/W] B,H,W 00000000* ⁴	
000F1C _H	—	—	—	—	Reserved
000F20 _H	PODR00[R/W] B,H,W 00000000	PODR01[R/W] B,H,W 00000000	PODR02[R/W] B,H,W 00000000	PODR03[R/W] B,H,W 00000000	Port output drive register *4:CY91F578/9 only
000F24 _H	PODR04[R/W] B,H,W 00000000	PODR05[R/W] B,H,W 00000000	PODR06[R/W] B,H,W 00000000	PODR07[R/W] B,H,W 00000000	
000F28 _H	PODR08[R/W] B,H,W 00000000	PODR09[R/W] B,H,W 00000000	PODR10[R/W] B,H,W 00000000	PODR11[R/W] B,H,W 00000000	
000F2C _H	PODR12[R/W] B,H,W 00000000	PODR13[R/W] B,H,W 00-000000	PODR14[R/W] B,H,W 00000000* ⁴	PODR15[R/W] B,H,W 00000000* ⁴	
000F30 _H	PODR16[R/W] B,H,W 00000000* ⁴	PODR17[R/W] B,H,W 00000000* ⁴	PODR18[R/W] B,H,W 00000000* ⁴	PODR19[R/W] B,H,W 00000000* ⁴	
000F34 _H	—	EPODR01 [R/W] B,H,W 00000000	EPODR02 [R/W] B,H,W 00000000	EPODR03 [R/W] B,H,W -00000000	Extended Port output drive register
000F38 _H	EPODR06 [R/W] B,H,W 00000000	EPODR07 [R/W] B,H,W 00000000	EPODR08 [R/W] B,H,W 00000000	—	
000F3C _H	—	—	—	—	Reserved
000F40 _H	PORTEN [R/W] B,H,W -----0	—	—	—	Port input enable register
000F44 _H to 000F6C _H	—	—	—	—	Reserved
000F70 _H	RCRH0[W] H,W XXXXXXXX	RCRL0[W] B,H,W XXXXXXXX	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	Up/down counter 0
000F74 _H	CCR0[R/W] B,H 00000000 -0001000	—	—	CSR0[R/W] B 00000000	
000F78 _H to 000F7C _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000F80 _H	RCRH1[W] H,W XXXXXXXX	RCRL1[W] B,H,W XXXXXXXX	UDCRH1 [R] H,W 00000000	UDCRL1[R] B,H,W 00000000	Up/down counter 1
000F84 _H	CCR1[R/W] B,H 00000000 -0001000		—	CSR1[R/W] B 00000000	
000F88 _H to 000F8C _H	—	—	—	—	Reserved
000F90 _H	OCCP4 [R/W] W 00000000 00000000 00000000 00000000				Output compare 4,5
000F94 _H	OCCP5 [R/W] W 00000000 00000000 00000000 00000000				
000F98 _H	OCFS45 [R/W] B, H, W -----11	—	OCSH45 [R/W] B, H, W ---0--00	OCSL45[R/W] B, H, W 0000--00	
000F9C _H	—	—	—	—	Reserved
000FA0 _H	CPCLR2 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 2
000FA4 _H	TCDT2 [R/W] W 00000000 00000000 00000000 00000000				
000FA8 _H	TCCSH2 [R/W] B,H,W 0----00	TCCSL2 [R/W] B,H,W -1-00000	—	—	
000FAC _H	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 3
000FB0 _H	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
000FB4 _H	TCCSH3 [R/W] B,H,W 0----00	TCCSL3 [R/W] B,H,W -1-00000	—	—	
000FB8 _H	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 4
000FBC _H	TCDT4 [R/W] W 00000000 00000000 00000000 00000000				
000FC0 _H	TCCSH4 [R/W] B,H,W 0----00	TCCSL4 [R/W] B,H,W -1-00000	—	—	
000FC4 _H	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 5
000FC8 _H	TCDT5 [R/W] W 00000000 00000000 00000000 00000000				
000FCC _H	TCCSH5 [R/W]B,H,W 0----00	TCCSL5 [R/W]B,H,W -1-00000	—	—	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000FD0 _H	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 6,7
000FD4 _H	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FD8 _H	ICFS67 [R/W] B, H, W -----00	—	LSYNS1 [R/W] B,H,W ----0000	ICS67 [R/W] B, H, W 00000000	
000FDC _H	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 8,9
000FE0 _H	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FE4 _H	ICFS89 [R/W] B, H, W -----00	—	—	ICS89 [R/W] B, H, W 00000000	
000FE8 _H	IPCP10 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 10,11
000FEC _H	IPCP11 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FF0 _H	ICFS1011 [R/W] B, H, W -----00	—	—	ICS1011 [R/W] B, H, W 00000000	
000FF4 _H to 000FFC _H	—	—	—	—	Reserved
001000 _H	SACR [R/W] B,H,W -----0	PICD [R/W] B,H,W ---0011	—	—	Clock control
001004 _H to 00103C _H	—	—	—	—	Reserved
001040 _H	—	SGDER0 [R/W] B,H,W 00000000	SGCR0[R/W] B,H,W -0000-0- 000--000		Sound generator 0
001044 _H	SGAR0[R/W] B,H,W 00000000 00000000		SGFR0[R/W] B,H,W 00000000	SGNR0[R/W] B,H,W 00000000	
001048 _H	SGTCR0[R/W] B,H,W 00000000	SGIDR0[R/W] B,H,W 00000000	SGPCR0[R/W] B,H,W 00000000 11111111		
00104C _H	SGDMAR0[W] B,H,W 00000000 00000000 00000000 00000000				
001050 _H to 00105C _H	—	—	—	—	
001060 _H	—	SGDER1[R/W] B,H,W 00000000	SGCR1[R/W] B,H,W -0000-0- 000--000		Sound generator 1
001064 _H	SGAR1[R/W] B,H,W 00000000 00000000		SGFR1[R/W] B,H,W 00000000	SGNR1[R/W] B,H,W 00000000	
001068 _H	SGTCR1[R/W] B,H,W 00000000	SGIDR1[R/W] B,H,W 00000000	SGPCR1[R/W] B,H,W 00000000 11111111		
00106C _H	SGDMAR1[W] B,H,W 00000000 00000000 00000000 00000000				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
001070 _H to 00107C _H	—	—	—	—	Reserved
001080 _H	—	SGDER2[R/W] B,H,W 00000000	SGCR2[R/W] B,H,W -0000-0- 000--000		Sound generator 2
001084 _H	SGAR2[R/W] B,H,W 00000000 00000000		SGFR2[R/W] B,H,W 00000000	SGNR2[R/W] B,H,W 00000000	
001088 _H	SGTCR2[R/W] B,H,W 00000000	SGIDR2[R/W] B,H,W 00000000	SGPCR2[R/W] B,H,W 00000000 11111111		
00108C _H	SGDMAR2[W] B,H,W 00000000 00000000 00000000 00000000				
001090 _H to 00109C _H	—	—	—	—	
0010A0 _H	—	SGDER3[R/W] B,H,W 00000000	SGCR3[R/W] B,H,W -0000-0- 000--000		Sound generator 3
0010A4 _H	SGAR3[R/W] B,H,W 00000000 00000000		SGFR3[R/W] B,H,W 00000000	SGNR3[R/W] B,H,W 00000000	
0010A8 _H	SGTCR3[R/W] B,H,W 00000000	SGIDR3[R/W] B,H,W 00000000	SGPCR3[R/W] B,H,W	00000000 11111111	
0010AC _H	SGDMAR3[W] B,H,W 00000000 00000000 00000000 00000000				
0010B0 _H to 0010BC _H	—	—	—	—	Reserved
0010C0 _H	—	SGDER4[R/W] B,H,W 00000000	SGCR4[R/W] B,H,W -0000-0- 000--000		Sound generator 4
0010C4 _H	SGAR4[R/W] B,H,W 00000000 00000000		SGFR4[R/W] B,H,W 00000000	SGNR4[R/W] B,H,W 00000000	
0010C8 _H	SGTCR4[R/W] B,H,W 00000000	SGIDR4[R/W] B,H,W 00000000	SGPCR4[R/W] B,H,W 00000000 11111111		
0010CC _H	SGDMAR4[W] B,H,W 00000000 00000000 00000000 00000000				
0010D0 _H to 00112C _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
001130 _H	—	—	—	CRCCR[R/W] B,H,W -0000000	CRC operation
001134 _H	CRCINIT[R/W] B,H,W 11111111 11111111 11111111 11111111				
001138 _H	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
00113C _H	CRCR[R] B,H,W 11111111 11111111 11111111 11111111				
001140 _H to 001FFC _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002000 _H	CTRLR0 [R/W] B,H,W -----000-0001		STATR0[R/W] B,H,W ----- 00000000		CAN0 (64msb)
002004 _H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008 _H	INTR0 [R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W ----- X00000--		
00200C _H	BRPER0 [R/W] B,H,W ----- ----0000		—		
002010 _H	IF1CREQ0 [R/W] B,H,W 0----- 00000001		IF1CMSK0 [R/W] B,H,W ----- 00000000		
002014 _H	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018 _H	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
00201C _H	IF1MCTR0 [R/W] B,H,W 00000000 0---0000		—		
002020 _H	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024 _H	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		
002028 _H , 00202C _H	Reserved				
002030 _H , 002034 _H	Reserved (IF1 data mirror)				
002038 _H , 00203C _H	Reserved				
002040 _H	IF2CREQ0 [R/W] B,H,W 0----- 00000001		IF2CMSK0 [R/W] B,H,W ----- 00000000		
002044 _H	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048 _H	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		
00204C _H	IF2MCTR0 [R/W] B,H,W 00000000 0---0000		—		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002050 _H	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		CAN0 (64msb)
002054 _H	IF2DTB10 [R/W] B,H,W 00000000 00000000		IF2DTB20 [R/W] B,H,W 00000000 00000000		
002058 _H , 00205C _H	Reserved				
002060 _H , 002064 _H	Reserved (IF2 data mirror)				
002068 _H to 00207C _H	Reserved				
002080 _H	TREQR20 [R] B,H,W 00000000 00000000		TREQR10 [R] B,H,W 00000000 00000000		
002084 _H	TREQR40 [R] B,H,W 00000000 00000000		TREQR30 [R] B,H,W 00000000 00000000		
002088 _H	—		—		
00208C _H	—		—		
002090 _H	NEWDT20 [R] B,H,W 00000000 00000000		NEWDT10 [R] B,H,W 00000000 00000000		
002094 _H	NEWDT40 [R] B,H,W 00000000 00000000		NEWDT30 [R]B,H,W 00000000 00000000		
002098 _H	—		—		
00209C _H	—		—		
0020A0 _H	INTPND20 [R] B,H,W 00000000 00000000		INTPND10 [R] B,H,W 00000000 00000000		
0020A4 _H	INTPND40 [R] B,H,W 00000000 00000000		INTPND30 [R] B,H,W 00000000 00000000		
0020A8 _H	—		—		
0020AC _H	—		—		
0020B0 _H	MSGVAL20 [R] B,H,W 00000000 00000000		MSGVAL10 [R] B,H,W 00000000 00000000		
0020B4 _H	MSGVAL40 [R] B,H,W 00000000 00000000		MSGVAL30 [R] B,H,W 00000000 00000000		
0020B8 _H	—		—		
0020BC _H	—		—		
0020C0 _H to 0020FC _H	Reserved				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002100 _H	CTRLR1 [R/W] B,H,W -----000-0001		STATR1[R/W] B,H,W ----- 00000000		CAN1 (32msb)
002104 _H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1[R/W] B,H,W -0100011 00000001		
002108 _H	INTR1 [R] B,H,W 00000000 00000000		TESTR1[R/W] B,H,W ----- X00000--		
00210C _H	BRPER1 [R/W] B,H,W ----- ----0000		—		
002110 _H	IF1CREQ1 [R/W] B,H,W 0----- 00000001		IF1CMSK1 [R/W] B,H,W ----- 00000000		
002114 _H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118 _H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211C _H	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—		
002120 _H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124 _H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128 _H , 00212C _H	Reserved				
002130 _H , 002134 _H	Reserved (IF1 data mirror)				
002138 _H , 00213C _H	Reserved				
002140 _H	IF2CREQ1 [R/W] B,H,W 0----- 00000001		IF2CMSK1 [R/W] B,H,W ----- 00000000		
002144 _H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148 _H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
00214C _H	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002150 _H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		CAN1 (32msb)
002154 _H	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		
002158 _H , 00215C _H	Reserved				
002160 _H , 002164 _H	Reserved (IF2 data mirror)				
002168 _H to 00217C _H	Reserved				
002180 _H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		
002184 _H	—		—		
002188 _H	—		—		
00218C _H	—		—		
002190 _H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		
002194 _H	—		—		
002198 _H	—		—		
00219C _H	—		—		
0021A0 _H	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
0021A4 _H	—		—		
0021A8 _H	—		—		
0021AC _H	—		—		
0021B0 _H	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
0021B4 _H	—		—		
0021B8 _H	—		—		
0021BC _H	—		—		
0021C0 _H to 0021FC _H	Reserved				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002200 _H	CTRLR2 [R/W] B,H,W ----- 000-0001		STATR2[R/W] B,H,W ----- 00000000		CAN2 (32msb)
002204 _H	ERRCNT2[R] B,H,W 00000000 00000000		BTR2[R/W] B,H,W -0100011 00000001		
002208 _H	INTR2[R] B,H,W 00000000 00000000		TESTR2[R/W] B,H,W ----- X00000--		
00220C _H	BRPER2 [R/W] B,H,W ----- ----0000		—		
002210 _H	IF1CREQ2[R/W] B,H,W 0----- 00000001		IF1CMSK2[R/W] B,H,W ----- 00000000		
002214 _H	IF1MSK22 [R/W] B,H,W 11-11111 11111111		IF1MSK12[R/W] B,H,W 11111111 11111111		
002218 _H	IF1ARB22 [R/W] B,H,W 00000000 00000000		IF1ARB12[R/W] B,H,W 00000000 00000000		
00221C _H	IF1MCTR2[R/W] B,H,W 00000000 0---0000		—		
002220 _H	IF1DTA12 [R/W] B,H,W 00000000 00000000		IF1DTA22[R/W] B,H,W 00000000 00000000		
002224 _H	IF1DTB12 [R/W] B,H,W 00000000 00000000		IF1DTB22[R/W] B,H,W 00000000 00000000		
002228 _H , 00222C _H	Reserved				
002230 _H , 002234 _H	Reserved (IF1 data mirror)				
002238 _H , 00223C _H	Reserved				
002240 _H	IF2CREQ2[R/W] B,H,W 0----- 00000001		IF2CMSK2[R/W] B,H,W ----- 00000000		
002244 _H	IF2MSK22 [R/W] B,H,W 11-11111 11111111		IF2MSK12[R/W] B,H,W 11111111 11111111		
002248 _H	IF2ARB22[R/W] B,H,W 00000000 00000000		IF2ARB12[R/W] B,H,W 00000000 00000000		
00224C _H	IF2MCTR2[R/W] B,H,W 00000000 0---0000		—		
002250 _H	IF2DTA12[R/W] B,H,W 00000000 00000000		IF2DTA22[R/W] B,H,W 00000000 00000000		
002254 _H	IF2DTB12[R/W] B,H,W 00000000 00000000		IF2DTB22[R/W] B,H,W 00000000 00000000		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002258 _H , 00225C _H	Reserved				CAN2 (32msb)
002260 _H , 002264 _H	Reserved (IF2 data mirror)				
002268 _H to 00227C _H	Reserved				
002280 _H	TREQR22[R] B,H,W 00000000 00000000		TREQR12[R] B,H,W 00000000 00000000		
002284 _H	—		—		
002288 _H	—		—		
00228C _H	—		—		
002290 _H	NEWDT22[R] B,H,W 00000000 00000000		NEWDT12[R] B,H,W 00000000 00000000		
002294 _H	—		—		
002298 _H	—		—		
00229C _H	—		—		
0022A0 _H	INTPND22[R] B,H,W 00000000 00000000		INTPND12[R] B,H,W 00000000 00000000		
0022A4 _H	—		—		
0022A8 _H	—		—		
0022AC _H	—		—		
0022B0 _H	MSGVAL22[R] B,H,W 00000000 00000000		MSGVAL12[R] B,H,W 00000000 00000000		
0022B4 _H	—		—		
0022B8 _H	—		—		
0022BC _H	—		—		
0022C0 _H to 0022FC _H	—	—	—	—	
002300 _H	DFCTLR[R/W] B,H,W -0-----		—	DFSTR[R/W] B,H,W -----001	WorkFlash
002304 _H	—	—	—	—	
002308 _H	FLIFCTLR [R/W] B,H,W ---0--00	—	FLIFFER1 [R/W] B,H,W -----	FLIFFER2 [R/W] B,H,W -----	Flash/ WorkFlash
00230C _H to 0023FC _H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002400 _H	SEEARX[R] B,H,W --000000 00000000 -0000000 00000000 ^{*4}		DEEARX[R] B,H,W --000000 00000000 -0000000 00000000 ^{*4}		XBS RAM ECC control register *4: CY91F578/9 only
002404 _H	EECSR[X/R/W] B,H,W ----0000	—	EFEARX [R/W] B,H,W --000000 00000000 -0000000 00000000 ^{*4}		
002408 _H	—		EFECRX [R/W] B,H,W -----0 00000000 00000000		
00240C _H to 002FFC _H	—	—	—	—	Reserved
003000 _H	SEEARA[R] B,H,W ----000 00000000 ----0000 00000000 ^{*4}		DEEARA[R] B,H,W ----000 00000000 ----0000 00000000 ^{*4}		Backup RAM ECC control register *4: CY91F578/9 only
003004 _H	EECSRA[R/W] B,H,W ----0000	—	EFEARA[R/W] B,H,W ----000 00000000 ----0000 00000000 ^{*4}		
003008 _H	—		EFECRA [R/W] B,H,W -----0 00000000 00000000		
00300C _H to 003FFC _H	—	—	—	—	Reserved
004000 _H to 007FFC _H	Backup-RAM ⁵				Backup RAM area
008000 _H to 00FEFC _H	—	—	—	—	Reserved (00F00 _H to[S])
00FF00 _H	DSUCR [R/W] B,H,W -----0		—	—	OCDU [S]
00FF04 _H to 00FF0C _H	—	—	—	—	Reserved [S]
00FF10 _H	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF14 _H	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00FF18 _H to 00FFF4 _H	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
00FFF8 _H	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FFFC _H	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated when read/write is performed on these registers in the user mode.

*3: The initial value is different by part number. For details, refer to the CSVCR register in chapter “Clock Supervisor”

*4: CY91F578/9 only

*5: See the maximum size of series on the memory map

12. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

Interrupt Vector

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN _{*1}
	Decimal	Hexa-decimal				
Reset	0	00	-	3FC _H	000FFFFC _H	-
System reserved	1	01	-	3F8 _H	000FFFF8 _H	-
System reserved	2	02	-	3F4 _H	000FFFF4 _H	-
System reserved	3	03	-	3F0 _H	000FFFF0 _H	-
System reserved	4	04	-	3EC _H	000FFFE _C	-
FPU exception	5	05	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	06	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	07	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	08	-	3DC _H	000FFFD _C	-
INTE instruction	9	09	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System Reserved	11	0B	-	3D0 _H	000FFFD0 _H	-
System Reserved	12	0C	-	3CC _H	000FFFC _C	-
System Reserved	13	0D	-	3C8 _H	000FFFC8 _H	-
Exception of illegal instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request/ XBS RAM double-bit error detection/ Backup RAM double-bit error detection	15	0F	15 (F _H) Fixed	3C0 _H	000FFFC0 _H	-
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFB _C	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFFB8 _H	1
Reload timer 0/1/4/5	18	12	ICR02	3B4 _H	000FFFB4 _H	2(*2)
Reload timer 2/3/6	19	13	ICR03	3B0 _H	000FFFB0 _H	3(*2)
Multi-function serial interface ch.0 (reception completed)/ Multi-function serial interface ch.0 (status)	20	14	ICR04	3AC _H	000FFFA _C	4 (*3)
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5
Multi-function serial interface ch.1 (reception completed)/ Multi-function serial interface ch.1 (status)	22	16	ICR06	3A4 _H	000FFFA4 _H	6 (*3)
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	3A0 _H	000FFFA0 _H	7
LIN-UART2 (reception completed)	24	18	ICR08	39C _H	000FFF9 _C	8
LIN-UART2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9
LIN-UART3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN *1
	Decimal	Hexa-decimal				
LIN-UART3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11
LIN-UART4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12
LIN-UART4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
LIN-UART5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14
LIN-UART5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15
LIN-UART6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16
LIN-UART6 (transmission completed)	33	21	ICR17	378 _H	000FFF78 _H	17
CAN0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN1	35	23	ICR19	370 _H	000FFF70 _H	-
CAN2/ Up/down counter 0/ Up/down counter 1	36	24	ICR20	36C _H	000FFF6C _H	-
Real time clock	37	25	ICR21	368 _H	000FFF68 _H	-
Sound generator 0 / LIN-UART7 (reception completed)	38	26	ICR22	364 _H	000FFF64 _H	22
Sound generator 1 / LIN-UART7 (transmission completed)	39	27	ICR23	360 _H	000FFF60 _H	23
PPG0/1/10/11/20/21	40	28	ICR24	35C _H	000FFF5C _H	24
PPG2/3/12/13/22/23	41	29	ICR25	358 _H	000FFF58 _H	25
PPG4/5/14/15	42	2A	ICR26	354 _H	000FFF54 _H	26
PPG6/7/16/17	43	2B	ICR27	350 _H	000FFF50 _H	27
PPG8/9/18/19	44	2C	ICR28	34C _H	000FFF4C _H	28
Multi-function serial interface ch.8 (reception completed)/ Multi-function serial interface ch.8 (status) / HS_SPI reception interrupt request	45	2D	ICR29	348 _H	000FFF48 _H	29 (*4)
Main timer/Sub timer/PLL timer / Multi-function serial interface ch.8(transmission completed)/ HS_SPI transmission interrupt request	46	2E	ICR30	344 _H	000FFF44 _H	30 (*4)
Clock calibration unit (Sub oscillation) / Sound generator 4/ Multi-function serial interface ch.9 (reception completed) / Multi-function serial interface ch.9 (status)	47	2F	ICR31	340 _H	000FFF40 _H	31 (*5)
A/D converter	48	30	ICR32	33C _H	000FFF3C _H	32
Clock calibration Unit (CR oscillation) / Multi-function serial interface ch.9 (transmission completed)	49	31	ICR33	338 _H	000FFF38 _H	33 (*5)
Free-run timer 0/2/4	50	32	ICR34	334 _H	000FFF34 _H	-
Free-run timer 1/3/5	51	33	ICR35	330 _H	000FFF30 _H	-
ICU0/6 (fetching)	52	34	ICR36	32C _H	000FFF2C _H	36
ICU1/7 (fetching)	53	35	ICR37	328 _H	000FFF28 _H	37
ICU2/8 (fetching)	54	36	ICR38	324 _H	000FFF24 _H	38
ICU3/9 (fetching)	55	37	ICR39	320 _H	000FFF20 _H	39
ICU4/10 (fetching)	56	38	ICR40	31C _H	000FFF1C _H	40
ICU5/11 (fetching)	57	39	ICR41	318 _H	000FFF18 _H	41

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN *1
	Decimal	Hexa-decimal				
OCU0/1/6/7/10/11 (match)	58	3A	ICR42	314 _H	000FFF14 _H	42
OCU2/3/4/5/8/9 (match)	59	3B	ICR43	310 _H	000FFF10 _H	43
Base timer 0 IRQ0 / Base timer 0 IRQ1 / Sound generator 2	60	3C	ICR44	30C _H	000FFF0C _H	44
Base timer 1 IRQ0 / Base timer 1 IRQ1 / Sound generator 3 / XBS RAM single bit error generation / Backup RAM single bit error generation	61	3D	ICR45	308 _H	000FFF08 _H	45 (*6)
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304 _H	000FFF04 _H	-
Delayed interrupt	63	3F	ICR47	300 _H	000FFF00 _H	-
System reserved (Used for REALOS™*7.)	64	40	-	2FC _H	000FFEFC _H	-
System reserved (Used for REALOS.)	65	41	-	2F8 _H	000FFE8 _H	-
Used with the INT instruction.	66	42	-	2F4 _H	000FEF4 _H	-
	 255	 FF		 000 _H	 000FFC00 _H	

- *1: It does not support the DMA transfer request by the interrupt generated from a peripheral to which no RN (Resource Number) is assigned.
- *2: Reload timer ch.4 to ch.6 does not support the DMA transfer by the interrupt.
- *3: The status of the multi-function serial interface does not support the DMA transfer by I²C reception.
- *4: HS_SPI does not support the DMA transfer by the interrupt.
- *5: The clock calibration unit does not support the DMA transfer by the interrupt.
- *6: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.
- *7: REALOS is the trademark of Cypress.

13. Electrical Characteristics

13.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	V _{CC5}	V _{SS} -0.3	V _{SS} +6.0	V	
	DV _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	DV _{CC} ≤ V _{CC5}
	V _{CC} E	V _{SS} -0.3	V _{SS} +6.0	V	V _{CC} E ≤ V _{CC5}
Analog power supply voltage*1,*2	AV _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	AVRH ≤ AV _{CC} ≤ V _{CC5}
Analog reference voltage*1	AVRH	V _{SS} -0.3	V _{SS} +6.0	V	AVRH ≤ AV _{CC}
Input voltage*1	V _{I1}	V _{SS} -0.3	V _{CC5} +0.3	V	
	V _{I2}	V _{SS} -0.3	V _{CC5} +0.3	V	SMC shared pin
	V _{IE}	V _{SS} -0.3	V _{CC5} +0.3	V	
Analog pin input voltage*1	V _{IA5}	V _{SS} -0.3	V _{CC5} +0.3	V	
Output voltage*1	V _{O1}	V _{SS} -0.3	V _{CC5} +0.3	V	
	V _{O2}	V _{SS} -0.3	V _{CC5} +0.3	V	SMC shared pin
	V _{OE}	V _{SS} -0.3	V _{CC5} +0.3	V	
Maximum clamp current	I _{CLAMP}	-4	4	mA	*8
Total maximum clamp current	Σ I _{CLAMP}	—	20	mA	*8
"L" level maximum output current *3	I _{OL1}	—	7	mA	2 mA is selected*6
	I _{OL2}	—	40	mA	30 mA is selected *7
"L" level average output current *4	I _{OLAV1}	—	2	mA	2 mA is selected *6
	I _{OLAV2}	—	30	mA	30 mA is selected *7
"L" level total output current*5	ΣI _{OL1}	—	50	mA	*6
	ΣI _{OL2}	—	250	mA	*7
"H" level maximum output current*3	I _{OH1} *3	—	-7	mA	2 mA is selected*6
	I _{OH2} *3	—	-40	mA	30 mA is selected *7
"H" level average output current*4	I _{OHAV1} *4	—	-2	mA	2 mA is selected *6
	I _{OHAV2} *4	—	-30	mA	30 mA is selected *7
"H" level total output current*5	ΣI _{OH1}	—	-50	mA	*6
	ΣI _{OH2}	—	-250	mA	*7
Power consumption	P _D	—	710	mW	
Operating temperature	T _A	-40	+105	°C	
Storage temperature	T _{stg}	-55	+150	°C	

*1: This parameter is based on V_{SS} = AV_{SS} = DV_{SS} = 0.0 V.

*2: Caution must be taken that AV_{CC}, DV_{CC}, and V_{CC}E do not exceed V_{CC5} upon power-on and under other circumstances.

*3: Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

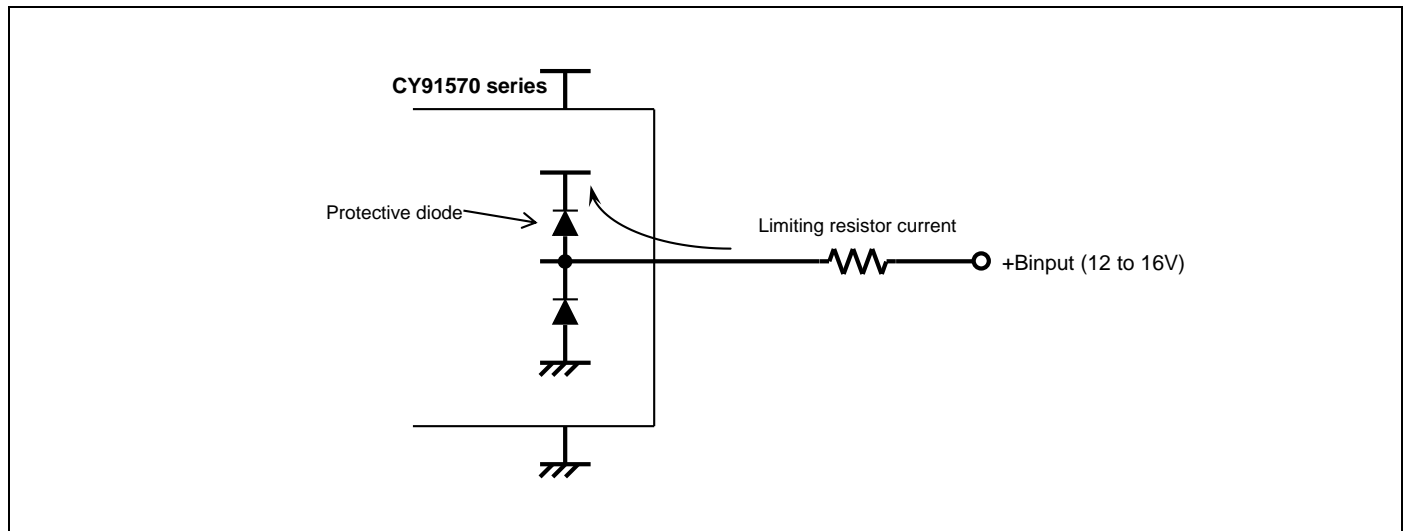
*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Outputs other than P60-P87 pins

*7: Output of P60-P87 pins

- *8:
- Corresponding pins: all general-purpose ports. (Except P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P053, P90/ADTG/PPGO_2)
 - Use within recommended operating conditions.
 - Use at DC voltage (current).
 - The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
 - The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
 - Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
 - Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
 - Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
 - Do not leave + B input pins open.

Sample Recommended Circuit



WARNING:

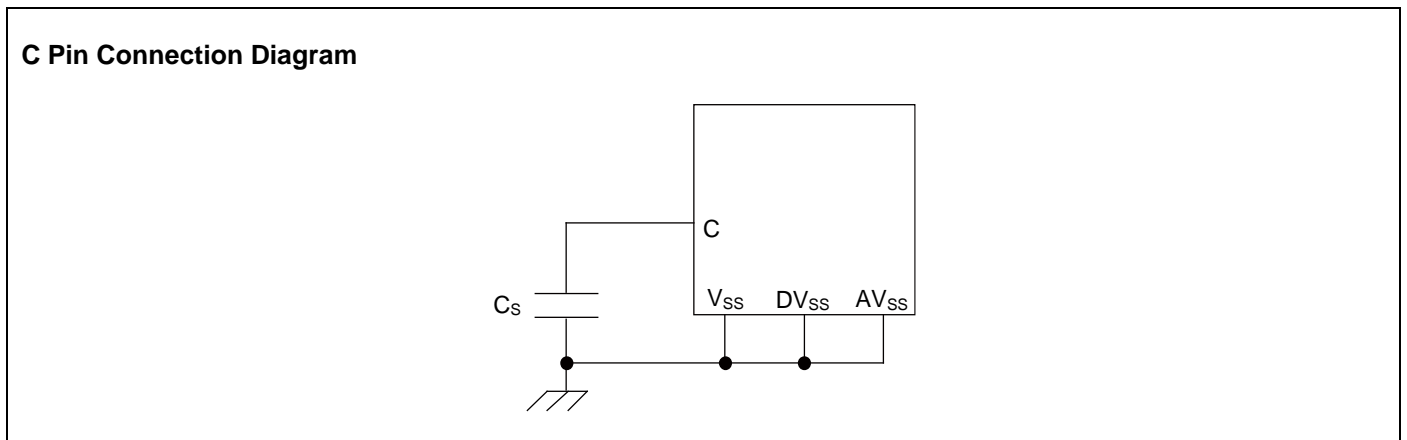
Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

13.2 Recommended Operating Conditions

(V_{SS} = DV_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V _{CC5}	4.5	5.5	V	Recommended operation guarantee range
	DV _{CC}	4.5	5.5	V	
	AV _{CC5}	4.5	5.5	V	
	V _{CC} E	3.0	5.5	V	
	V _{CC5}	3.5	5.5	V	Operation guarantee range
	DV _{CC}	3.5	5.5	V	
	AV _{CC5}	3.5	5.5	V	
	V _{CC} E	2.7	5.5	V	
Smoothing capacitor *	C _S	4.7 (tolerance within ±50%)		μF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C _S as the smoothing capacitor on the V _{CC} pin.
Operating temperature	T _A	-40	+105	°C	

*: Refer to the following diagram for details on the connection of smoothing capacitor C_S.



WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions. Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

13.3 DC Characteristics

 (TA: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC E} = 5.0V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V _{IH1}	P010 to P017, P020 to P027, P030 to P036	CMOS input level is selected	0.7×V _{CC E}	—	V _{CC5} +0.3	V	*
	V _{IH2}		CMOS hysteresis input level is selected	0.7×V _{CC E}	—	V _{CC5} +0.3	V	*
	V _{IH3}		Automotive input level is selected	0.8×V _{CC E}	—	V _{CC5} +0.3	V	*
	V _{IH4}		TTL input level is selected	2.0	—	V _{CC5} +0.3	V	*
	V _{IH5}	P000 to P007, P037, P040 to P047, P050 to P057, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137, P140 to P147, P150 to P157, P160 to P167, P170 to P177, P180 to P187, P190 to P197 ^{*1}	CMOS input level is selected	0.7×V _{CC5}	—	V _{CC5} +0.3	V	
	V _{IH6}		CMOS hysteresis input level is selected	0.7×V _{CC5}	—	V _{CC5} +0.3	V	
	V _{IH7}		Automotive input level is selected	0.8×V _{CC5}	—	V _{CC5} +0.3	V	
	V _{IH8}		TTL input level is selected	2.0	—	V _{CC5} +0.3	V	
	V _{IH9}	RSTX, NMIX, MD2	—	0.7×V _{CC5}	—	V _{CC5} +0.3	V	
	V _{IH10}	MD0, MD1	—	0.7×V _{CC5}	—	V _{CC5} +0.3	V	
	V _{IH11}	DEBUGIF	—	2.0	—	V _{CC5} +0.3	V	

 *: V_{CC E} = 5.0V±10%, or V_{CC E} = 3.0 to 3.6V

*1: CY91F578/9 only supports P140 to P147, P150 to P157, P160 to P167, P170 to P177, P180 to P187, P190 to P197.

(TA: Recommended operating conditions, $V_{CC5} = 5.0 V \pm 10\%$, $V_{CC E} = 5.0 V \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V_{IL1}	P010 to P017, P020 to P027, P030 to P036	CMOS input level is selected	$V_{SS} - 0.3$	—	$0.3 \times V_{CC E}$	V	*
	V_{IL2}		CMOS hysteresis input level is selected	$V_{SS} - 0.3$	—	$0.3 \times V_{CC E}$	V	*
	V_{IL3}		Automotive input level is selected	$V_{SS} - 0.3$	—	$0.5 \times V_{CC E}$	V	*
	V_{IL4}		TTL input level is selected	$V_{SS} - 0.3$	—	0.8	V	*
	V_{IL5}	P000 to P007, P037, P040 to P047, P050 to P057, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137, P140 to P147, P150 to P157, P160 to P167, P170 to P177, P180 to P187, P190 to P197 ^{*1}	CMOS input level is selected	$V_{SS} - 0.3$	—	$0.3 \times V_{CC 5}$	V	
	V_{IL6}		CMOS hysteresis input level is selected	$V_{SS} - 0.3$	—	$0.3 \times V_{CC 5}$	V	
	V_{IL7}		Automotive input level is selected	$V_{SS} - 0.3$	—	$0.5 \times V_{CC 5}$	V	
	V_{IL8}		TTL input level is selected	$V_{SS} - 0.3$	—	0.8	V	
	V_{IL9}	RSTX, NMIX, MD2	—	$V_{SS} - 0.3$	—	$0.3 \times V_{CC 5}$	V	
	V_{IL10}	MD0, MD1	—	$V_{SS} - 0.3$	—	$0.3 \times V_{CC 5}$	V	
	V_{IL11}	DEBUGIF	—	$V_{SS} - 0.3$	—	0.8	V	

*: $V_{CC E} = 5.0V \pm 10\%$, or $V_{CC E} = 3.0$ to $3.6V$

*1: CY91F578/9 only supports P140 to P147, P150 to P157, P160 to P167, P170 to P177, P180 to P187, P190 to P197.

(TA: Recommended operating conditions, $V_{CC5} = 5.0V \pm 10\%$, $V_{CC E} = 5.0V \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P010 to P017, P020 to P027, P030 to P036	$V_{CC E} = 3.0 V$ $I_{OH} = -0.5 mA$	$V_{CC E}$ -0.5	—	$V_{CC E}$	V	*
	V_{OH2}		$V_{CC E} = 3.0 V$ $I_{OH} = -1.0 mA$	$V_{CC E}$ -0.5	—	$V_{CC E}$	V	*
	V_{OH3}		$V_{CC E} = 3.0 V$ $I_{OH} = -2.0 mA$	$V_{CC E}$ -0.5	—	$V_{CC E}$	V	*
	V_{OH4}	P000 to P007, P037, P040 to P047, P050 to P056, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137, P140 to P147, P150 to P157, P160 to P167, P170 to P177, P180 to P187, P190 to P197 ^{*1}	$V_{CC5} = 4.5 V$ $I_{OH} = -1.0 mA$	V_{CC5} -0.5	—	V_{CC5}	V	
	V_{OH5}		$V_{CC5} = 4.5 V$ $I_{OH} = -2.0 mA$	V_{CC5} -0.5	—	V_{CC5}	V	
	V_{OH6}	P060 to P067, P070 to P077, P080 to P087	$DV_{CC} = 4.5 V$ $I_{OH} = -30.0 mA$	DV_{CC} -0.5	—	DV_{CC}	V	SMC shared pin

*: $V_{CC E} = 5.0V \pm 10\%$, or $V_{CC E} = 3.0$ to $3.6V$

*1: CY91F578/9 only supports P140 to P147, P150 to P157, P160 to P167, P170 to P177, P180 to P187, P190 to P197.

(TA: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC E} = 5.0V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“L” level output voltage	V _{OL1}	P010 to P017, P020 to P027, P030 to P036	V _{CC E} = 3.0 V I _{OL} = 0.5 mA	0	—	0.4	V	*
	V _{OL2}		V _{CC E} = 3.0 V I _{OL} = 1.0 mA	0	—	0.4	V	*
	V _{OL3}		V _{CC E} = 3.0 V I _{OL} = 2.0 mA	0	—	0.4	V	*
	V _{OL4}	P000 to P007, P037, P040 to P047, P050 to P056, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137, P140 to P147, P150 to P157, P160 to P167, P170 to P177, P180 to P187, P190 to P197 ^{*1}	V _{CC5} = 4.5 V I _{OL} = 1.0 mA	0	—	0.4	V	
	V _{OL5}		V _{CC5} = 4.5 V I _{OL} = 2.0 mA	0	—	0.4	V	
	V _{OL6}	P060 to P067, P070 to P077, P080 to P087	DV _{CC} = 4.5 V I _{OL} = 30.0 mA	0	—	0.55	V	SMC shared pin
	V _{OL7}	P127, P130, P132, P133	V _{CC5} = 4.5 V I _{OL} = 3.0 mA	0	—	0.4	V	I ² C shared pin (I ² C is selected)
	V _{OL8}	DEBUGIF	V _{CC5} = 2.7 V I _{OL} = 25.0 mA	0	—	0.25	V	

*: V_{CC E} = 5.0V±10%, or V_{CC E} = 3.0 to 3.6V

*1: CY91F578/9 only supports P140 to P147, P150 to P157, P160 to P167, P170 to P177, P180 to P187, P190 to P197.

(TA: Recommended operating conditions, $V_{CC5} = 5.0V \pm 10\%$, $V_{CC E} = 5.0V \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{L1}	Port input pins other than P107,123	$V_{CC5} = V_{CC E} = DV_{CC} = AV_{CC} = 5.5 V$ $V_{SS} < V_I < V_{CC}$	-5	—	+5	μA	
	I_{L2}	P107, P123 (DA shared pin)		-10	—	+10	μA	
Pull-up resistance	R_{UP1}	RSTX, NMIX	—	25	—	100	k Ω	
	R_{UP2}	All port input pins	Pull-up resistance is selected	25	—	100	k Ω	
Pull-down resistance	R_{DOWN1}	MD2	—	25	—	100	k Ω	
	R_{DOWN2}	All port input pins	Pull-down resistance is selected	25	—	100	k Ω	
Input capacitance	C_{IN1}	Other than VCCE, V_{CC5} , V_{SS} , DV_{CC} , DV_{SS} , AV_{CC} , AV_{SS} , C, P060 to P067, P070 to P077, P080 to P087	—	—	5	15	pF	
	C_{IN2}	P060 to P067, P070 to P077, P080 to P087	When using SMC	—	15	45	pF	

(TA: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC E} = 5.0V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I _{CC5}	V _{CC5}	At normal operation Operating frequency F _{CP} = 80 MHz, F _{cpp} = 40 MHz	—	60	100	mA	*4
						125		*5
			FLASH write Operating frequency F _{CP} = 80 MHz, F _{cpp} = 40 MHz	—	75	115	mA	*3, *4
						140		*3, *5
			At FLASH erase Operating frequency F _{CP} = 80 MHz, F _{cpp} = 40 MHz	—	75	115	mA	*3, *4
						140		*3, *5
	I _{CCS5}		At sleep mode Operating frequency F _{CP} = 80 MHz, F _{cpp} = 40 MHz	—	20	60	mA	*4
						75		*5
	I _{CCBS5}		At bus sleep mode Operating frequency F _{CP} = 80 MHz, F _{cpp} = 40 MHz	—	15	55	mA	*4
						70		*5
	I _{CC T5}		At RTC mode 4MHz source oscillation	—	750	1400	μA	When using external clock*1, T _A = 25°C
				—		900		1550
I _{CC TS5}	At RTC mode shutdown 4MHz source oscillation	—	170	330	μA	When using external clock*1, T _A = 25°C		
		—		320		480	μA	When using crystal, T _A = 25°C
I _{CC H5}	At stop mode	—	400	1200	μA	T _A = 25°C		
I _{CC HS5}	At stop mode shutdown	—	120	240	μA	T _A = 25°C		

(T_A: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC6} = 5.0V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
High current output drive capacity Phase-to-phase deviation1	ΔV_{OH6}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn (n = 0 to 5)	DV _{CC} = 4.5 V I _{OH} = -30.0 mA Maximum deviation of V _{OH6}	—	—	90	mV	*2
High current output drive capacity Phase-to-phase deviation2	ΔV_{OL6}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn (n = 0 to 5)	DV _{CC} = 4.5 V I _{OL} = 30.0 mA Maximum deviation of V _{OL6}	—	—	90	mV	*2
LCD divider resistor	R _{LCD}	V0 to V1, V1 to V2, V2 to V3	—	6.25	12.5	25	kΩ	
COM0 to COM3 output impedance	R _{VCOM}	COMm (m = 0 to 3)	—	—	—	4.5	kΩ	
SEG00 to SEG31 output impedance	R _{VSEG}	SEGn (n = 00 to 31)	—	—	—	17	kΩ	
LCDC leak current	I _{LCDC}	V0 to V3, COMm (m = 0 to 3), SEGn (n = 00 to 31)	T _A = +25°C	-0.5	—	+0.5	μA	

*1: The power supply current value when the external clock is supplied from the X1 pin. Note that the power supply current value when using the external clock is different from that using the oscillator.

*2: If PWM1P0/PWM1M0/PWM2P0/PWM2M0 of ch.0 is turned on simultaneously, the maximum deviation of V_{OH6} / V_{OL6} for each pin is defined. Same for other channels.

*3: This product contains both program flash and WorkFlash. This parameter is defined when only one of them is in the write/erase state.

*4: CY91F575/7

*5: CY91F578/9

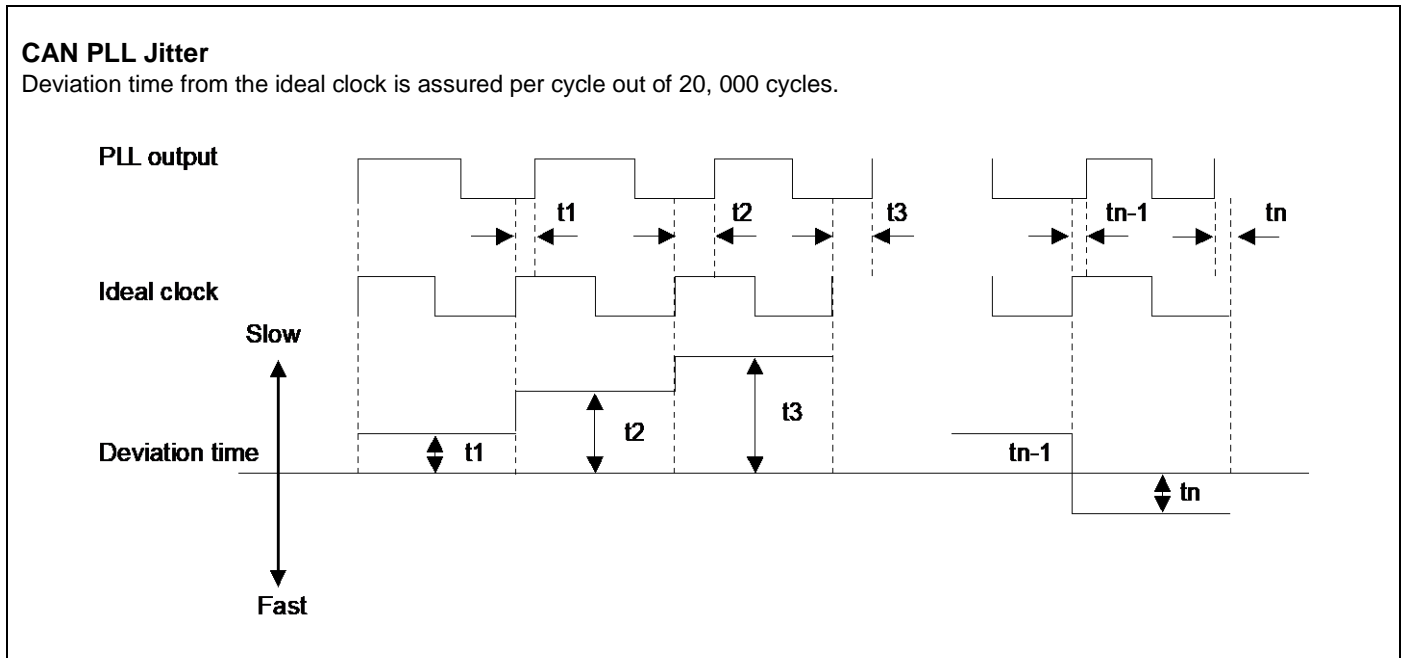
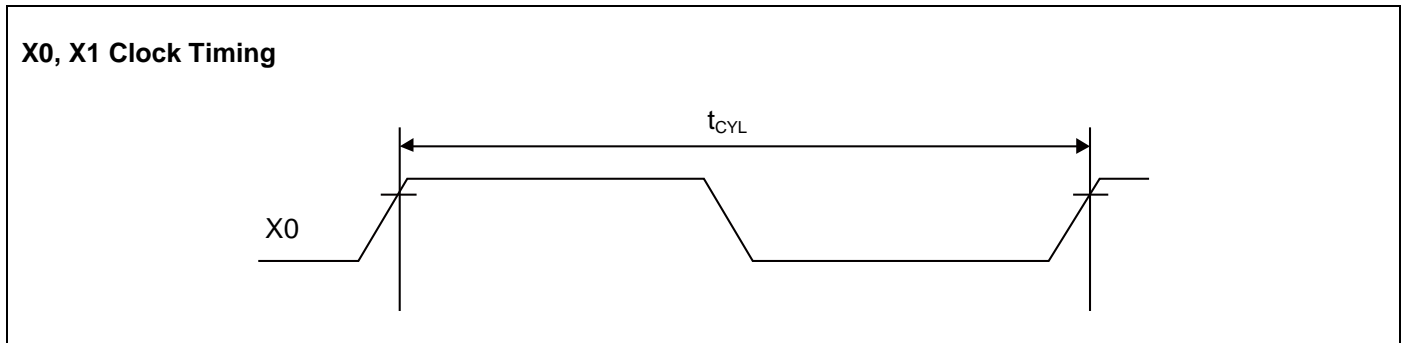
13.4 AC Characteristics

13.4.1 Main Clock Timing

(T_A: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F _C	X0, X1	–	–	4	–	MHz	
Source oscillation clock cycle time	t _{CYL}	X0, X1	–	–	250	–	ns	
Internal operating clock cycle time*	F _{CP}	–	–	2	–	80	MHz	CPU clock
	F _{CPP}	–	–	2	–	40	MHz	Peripheral bus clock
	F _{CPT}	–	–	2	–	40	MHz	External bus clock
Internal operating clock cycle time*	t _{CP}	–	–	12.5	–	500	ns	CPU clock
	t _{CPP}	–	–	25	–	500	ns	Peripheral bus clock
	t _{CPT}	–	–	25	–	500	ns	External bus clock
CAN PLL jitter (when lock)	t _{PJ}	–	–	-10	–	+10	ns	F _{CP} = 80 MHz (4 MHzxMultiplied by 20)
Built-in CR oscillation frequency	F _{CCR}	–	–	50	100	200	kHz	

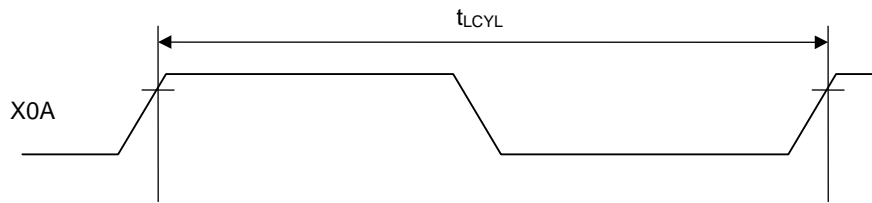
*: The maximum / minimum value is defined when using the main clock and PLL clock.



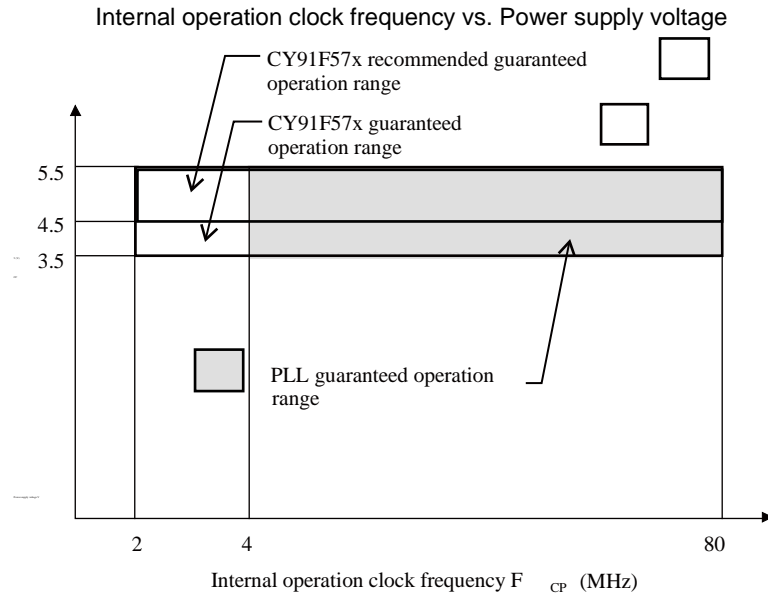
13.4.2 Sub Clock Timing (Products without S-suffix)

 (T_A: Recommended operating conditions, V_{CC} = 5.0V±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F _{CL}	X0A, X1A	–	–	32.768	–	kHz	
Source oscillation clock cycle time	t _{LCYL}	X0A, X1A	–	–	30.52	–	μs	

X0A, X1A Clock Timing


Guaranteed Operation Range

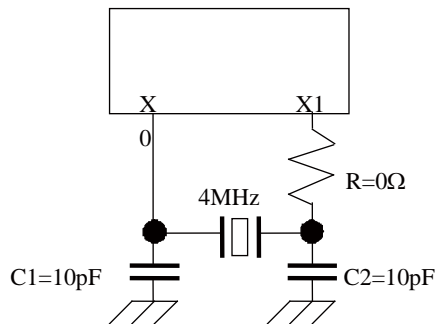


Note: The CPU will be reset at the power supply voltage $4V \pm 0.3V$ or less.

Oscillation Clock Frequency vs. Internal Operation Clock Frequency

		Internal Operation Clock Frequency							
		Main Clock	PLL Clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 19	Multiplied by 20
Oscillation clock frequency	4 MHz	2 MHz	4 MHz	8 MHz	12 MHz	16 MHz	...	76 MHz	80 MHz

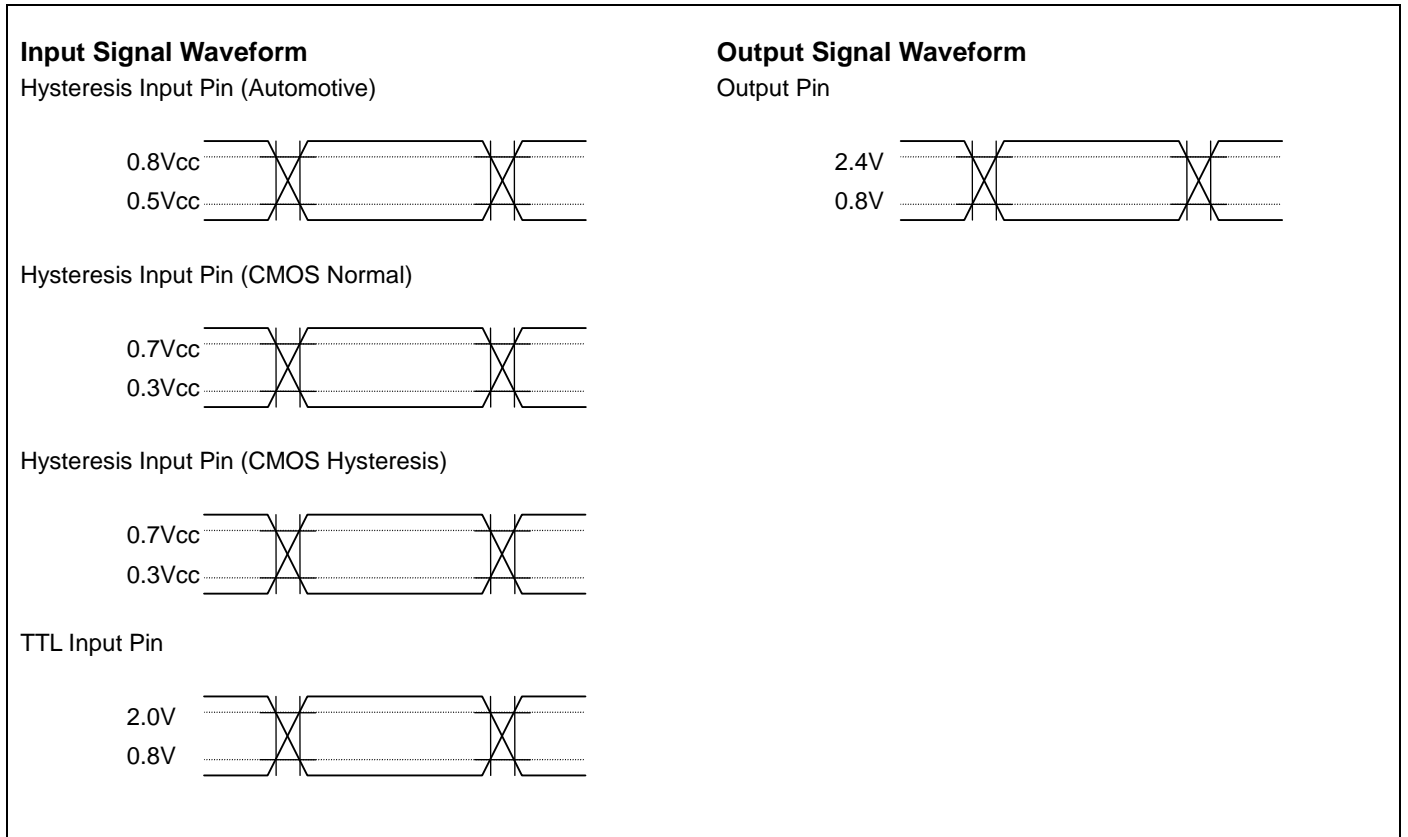
■ Example of oscillation circuit



Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.

Design your printed circuit board so that the oscillator can start oscillation within 20ms.

AC characteristics are specified by the following measurement reference voltage values.



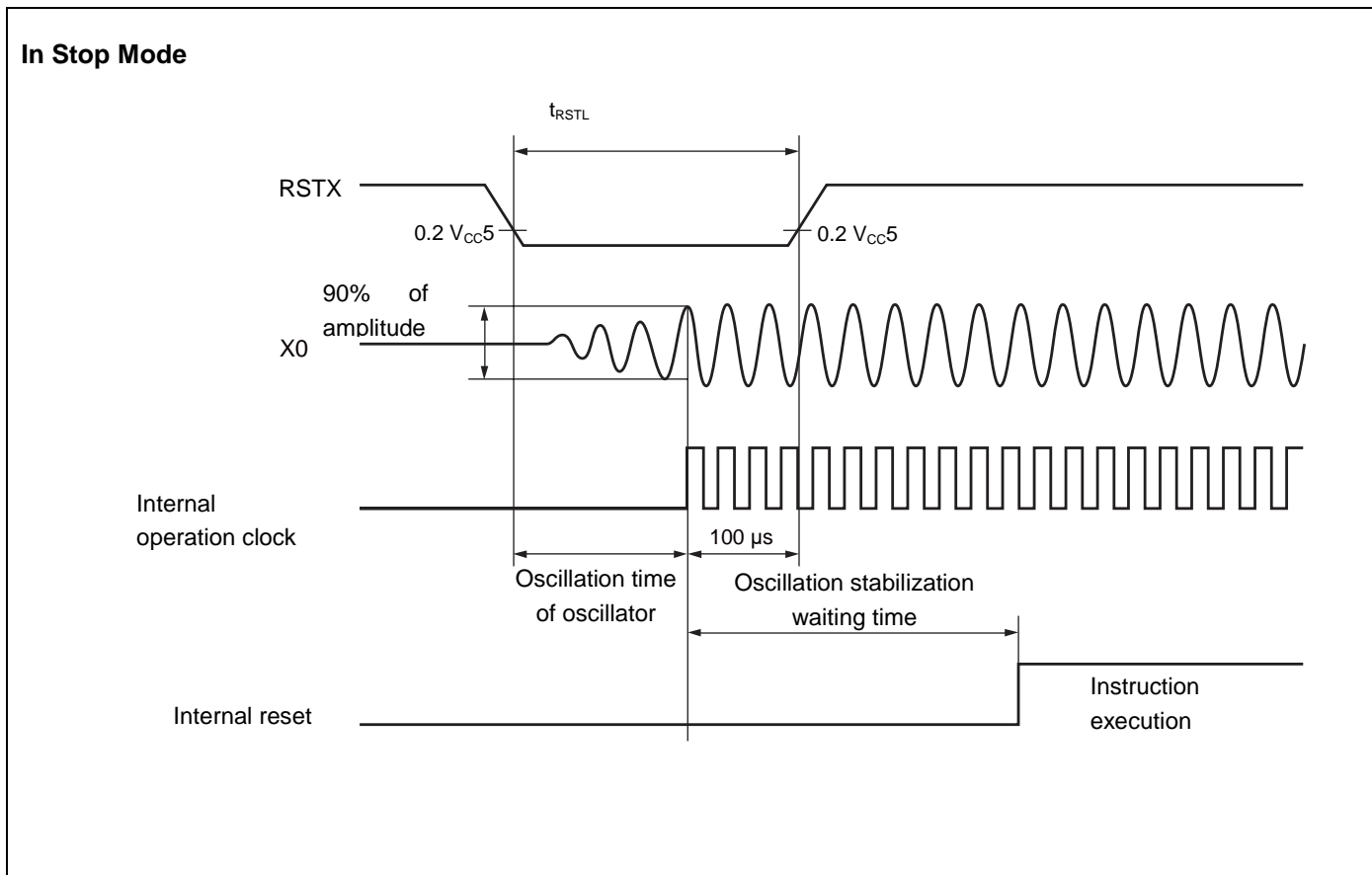
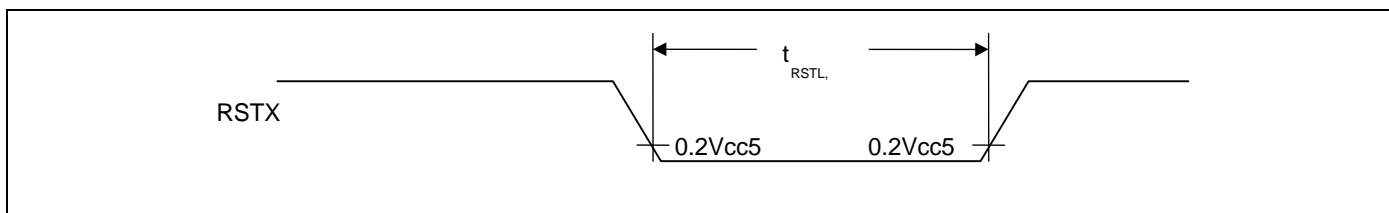
13.4.3 Reset Input

(T_A : Recommended operating conditions, $V_{CC5} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	—	10	—	μs	Under normal operation
				Oscillation time of oscillator* +100 μs	—	ms	In Stop mode
				100 μs	—	μs	In RTC mode
Width for reset input removal				1 μs	—	μs	

*: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%.

For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred μs and several ms, and for an external clock, the time is 0 ms.



13.4.4 Power-on Conditions

 (T_A: Recommended operating conditions, V_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	V _{CC5}	–	2.1	2.3	2.5	V	When turning on power for microcontroller
Level detection hysteresis width	–	V _{CC5}	–	–	–	125	mV	During voltage drop
Level detection time	–	–	–	–	–	30	us	*1
Slope detection undetected standard	–	V _{CC5}	V _{CC5} = at level detection release level time	–	–	4	mV/μs	*2
Power off time	t _{OFF}	V _{CC5}	–	50	–	–	ms	*3

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.

*3: This time is to start the slope detection at next power on after power down and internal charge loss

13.4.5 Multi-function Serial

13.4.5.1 UART Timing

Bit setting: SMR: MD2 = 0, SMR: MD1 = 1, SMR: MD0 = 0, SMR: SCINV = 0, SCR: SPI = 0

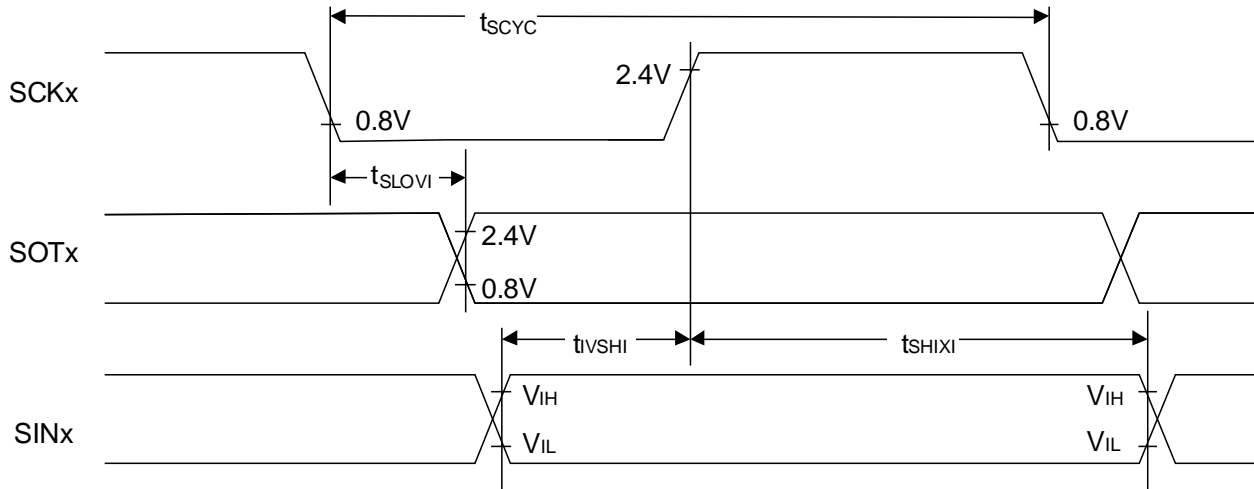
(T_A: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC E} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0, SCK1, SCK8, SCK9	—	4t _{CPP}	—	ns	Internal shift clock mode: C _L = 50 pF (When drive capability is 2 mA or more.) C _L = 20 pF (When drive capability is 1 mA)
SCK ↓→ SOT delay time	t _{SLOVI}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9		-30	+30	ns	
Valid SIN→ SCK ↑ setup time	t _{IVSHI}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		34	—	ns	
SCK ↑→ Valid SIN hold time	t _{SHIXI}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		0	—	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0, SCK1, SCK8, SCK9	—	t _{CPP} +10	—	ns	External shift clock mode: C _L = 50 pF (When drive capability is 2mA or more.) C _L = 20 pF (When drive capability is 1mA)
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	—	ns	
SCK ↓→ SOT delay time	t _{SLOVE}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9		—	33	ns	
Valid SIN→ SCK ↑setup time	t _{IVSHE}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		10	—	ns	
SCK ↑→ Valid SIN hold time	t _{SHIXE}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		20	—	ns	
SCK fall time	t _F	SCK0, SCK1, SCK8, SCK9		—	5	ns	
SCK rise time	t _R	SCK0, SCK1, SCK8, SCK9		—	5	ns	

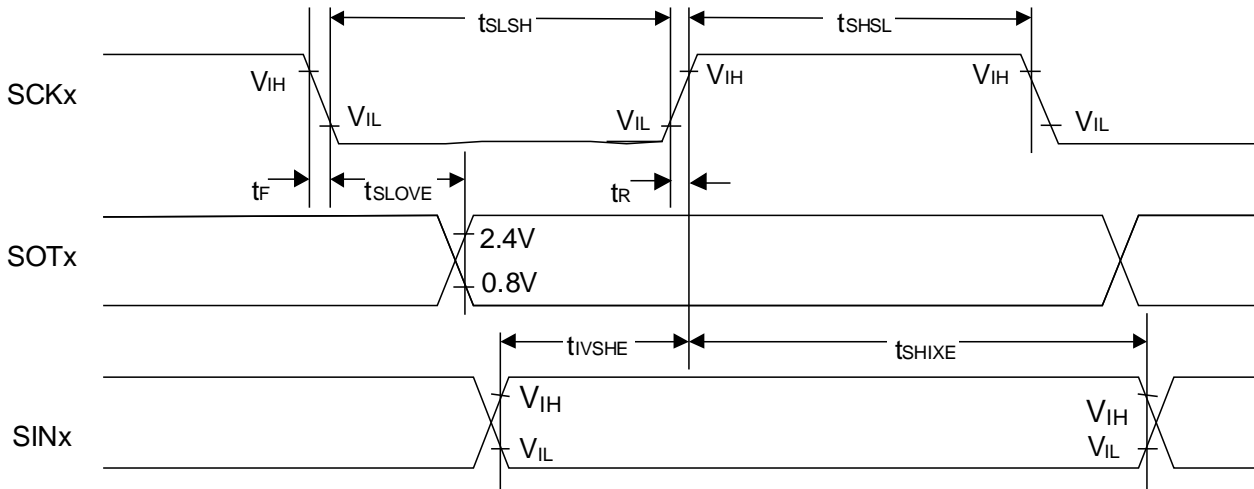
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. Refer to Hardware Manual for details.

• Internal shift clock mode



• External shift clock mode



Bit setting: SMR: MD2 = 0, SMR: MD1 = 1, SMR: MD0 = 0, SMR: SCINV = 1, SCR: SPI = 0

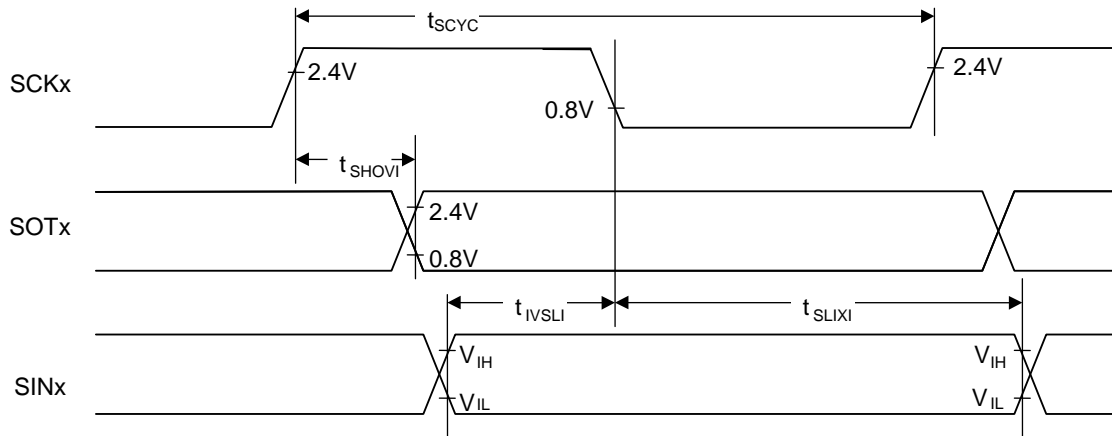
(TA: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC E} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0, SCK1, SCK8, SCK9	—	4t _{CPP}	—	ns	Internal shift clock mode: C _L = 50 pF (When drive capability is 2 mA or more.) C _L = 20 pF (When drive capability is 1 mA)
SCK ↑ → SOT delay time	t _{SHOVI}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9		-30	+30	ns	
Valid SIN → SCK ↓ setup time	t _{IVSLI}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		34	—	ns	
SCK ↓ → Valid SIN hold time	t _{SLIXI}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		0	—	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0, SCK1, SCK8, SCK9	—	t _{CPP} +10	—	ns	External shift clock mode: C _L = 50 pF (When drive capability is 2 mA or more.) C _L = 20 pF (When drive capability is 1 mA)
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	—	ns	
SCK ↑ → SOT delay time	t _{SHOVE}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9		—	33	ns	
Valid SIN → SCK ↓ setup time	t _{IVSLE}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		10	—	ns	
SCK ↓ → Valid SIN hold time	t _{SLIXE}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		20	—	ns	
SCK fall time	t _F	SCK0, SCK1, SCK8, SCK9		—	5	ns	
SCK rise time	t _R	SCK0, SCK1, SCK8, SCK9		—	5	ns	

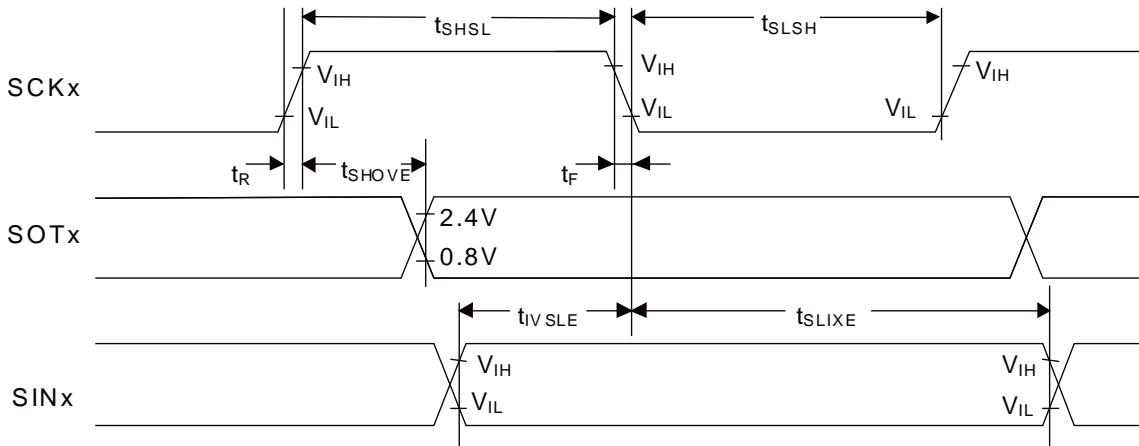
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. Refer to Hardware Manual for details.

Internal Shift Clock Mode



External Shift Clock Mode



Bit setting: SMR: MD2 = 0, SMR: MD1 = 1, SMR: MD0 = 0, SMR: SCINV = 0, SCR: SPI = 1

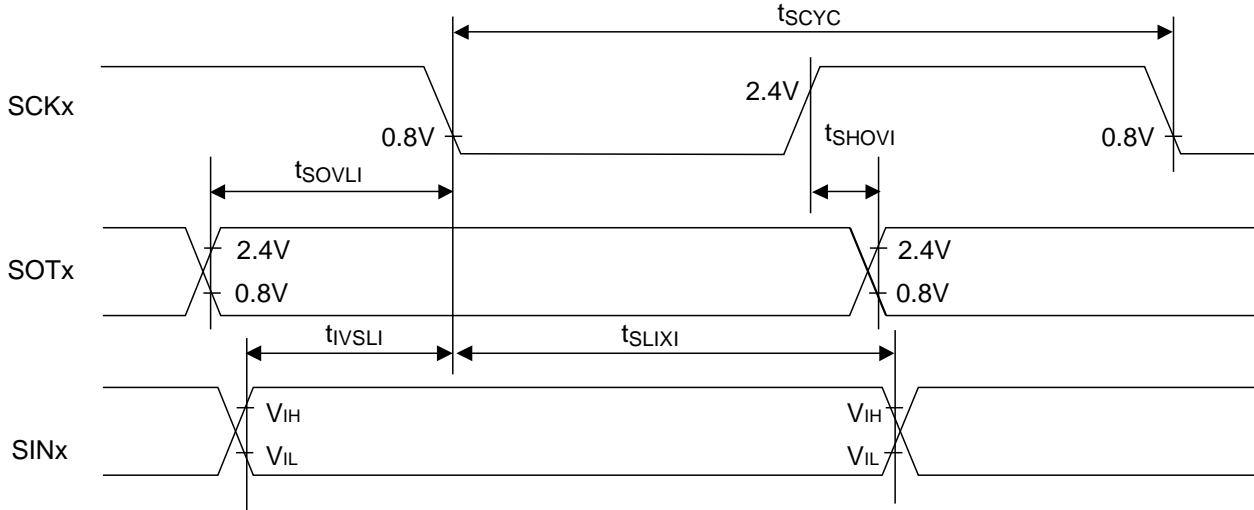
(TA: Recommended operating conditions, V_{CC5} = 5.0V ± 10%, V_{CC E} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Min	
Serial clock cycle time	t _{SCYC}	SCK0, SCK1, SCK8, SCK9	Internal shift clock mode C _L = 50 pF (When drive capability is 2 mA or more.) C _L = 20 pF (When drive capability is 1 mA)	4t _{CPP}	–	ns
SCK↑→SOT delay time	t _{SHOVI}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9		-30	+30	ns
Valid SIN→SCK↓ setup time	t _{IVSLI}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		34	–	ns
SCK↓→ Valid SIN hold time	t _{SLIXI}			0	–	ns
SOT→SCK↓ delay time	t _{SOVLI}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9		2t _{CPP} -30	–	ns
Serial clock "H" pulse width	t _{SHSL}	SCK0, SCK1, SCK8, SCK9		t _{CPP} +10	–	ns
Serial clock "L" pulse width	t _{SLSH}		2t _{CPP} -10	–	ns	
SCK↑→SOT delay time	t _{SHOVE}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9	External shift clock mode C _L = 50 pF (When drive capability is 2 mA or more.) C _L = 20 pF (When drive capability is 1 mA)	–	33	ns
Valid SIN→SCK↓ setup time	t _{IVSLE}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		10	–	ns
SCK↓→ Valid SIN hold time	t _{SLIXE}			20	–	ns
SCK fall time	t _F	SCK0, SCK1, SCK8, SCK9		–	5	ns
SCK rise time	t _R	SCK0, SCK1, SCK8, SCK9		–	5	ns

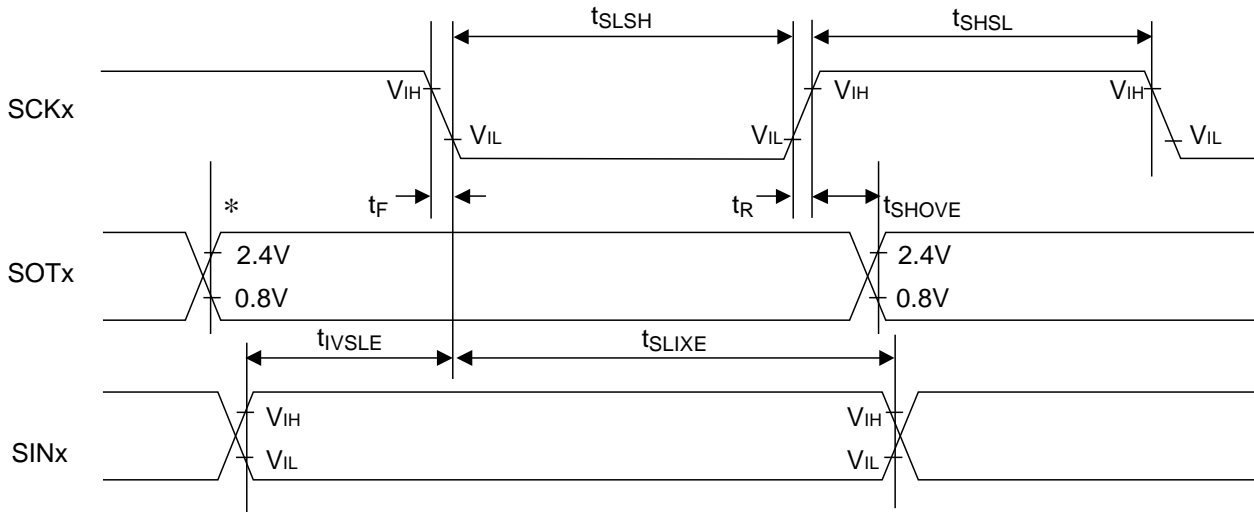
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters. Refer to Hardware Manual for details.

• Internal shift clock mode



• External shift clock mode



*: Changes when writing to TDR register

Bit setting: SMR: MD2 = 0, SMR: MD1 = 1, SMR: MD0 = 0, SMR: SCINV = 1, SCR: SPI = 1

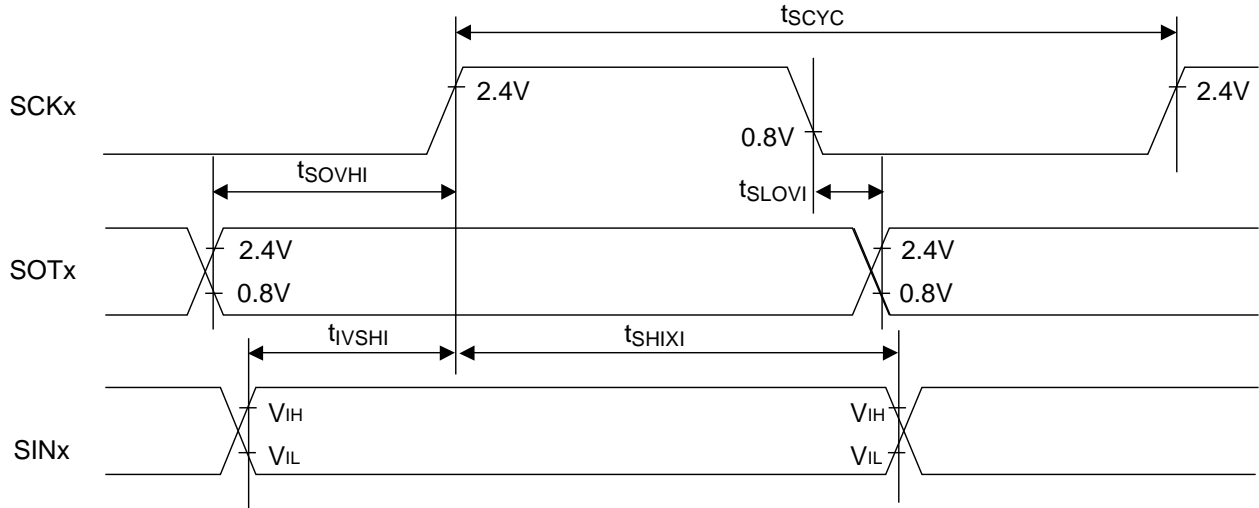
(TA: Recommended operating conditions, $V_{CC5} = 5.0V \pm 10\%$, $V_{CC E} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Min	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1, SCK8, SCK9	Internal shift clock mode $C_L = 50$ pF (When drive capability is 2 mA or more.) $C_L = 20$ pF (When drive capability is 1 mA)	$4t_{CPP}$	–	ns
SCK \downarrow →SOT delay time	t_{SLOVI}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9		-30	+30	ns
Valid SIN→SCK \uparrow setup time	t_{IVSHI}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		34	–	ns
SCK \uparrow → Valid SIN hold time	t_{SHIXI}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9		0	–	ns
SOT→SCK \uparrow delay time	t_{SOVHI}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9		$2t_{CPP}-30$	–	ns
Serial clock "H" pulse width	t_{SHSL}	SCK0, SCK1, SCK8, SCK9	External shift clock mode $C_L = 50$ pF (When drive capability is 2 mA or more.) $C_L = 20$ pF (When drive capability is 1 mA)	$t_{CPP}+10$	–	ns
Serial clock "L" pulse width	t_{SLSH}	SCK0, SCK1, SCK8, SCK9		$2t_{CPP}-10$	–	ns
SCK \downarrow →SOT delay time	t_{SLOVE}	SCK0, SCK1, SCK8, SCK9, SOT0, SOT1, SOT8, SOT9		–	33	ns
Valid SIN→SCK \uparrow setup time	t_{IVSHE}	SCK0, SCK1, SCK8, SCK9, SIN0, SIN1, SIN8, SIN9		10	–	ns
SCK \uparrow → Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SCK8, SCK9		20	–	ns
SCK fall time	t_F	SCK0, SCK1, SCK8, SCK9		–	5	ns
SCK rise time	t_R	SCK0, SCK1, SCK8, SCK9		–	5	ns

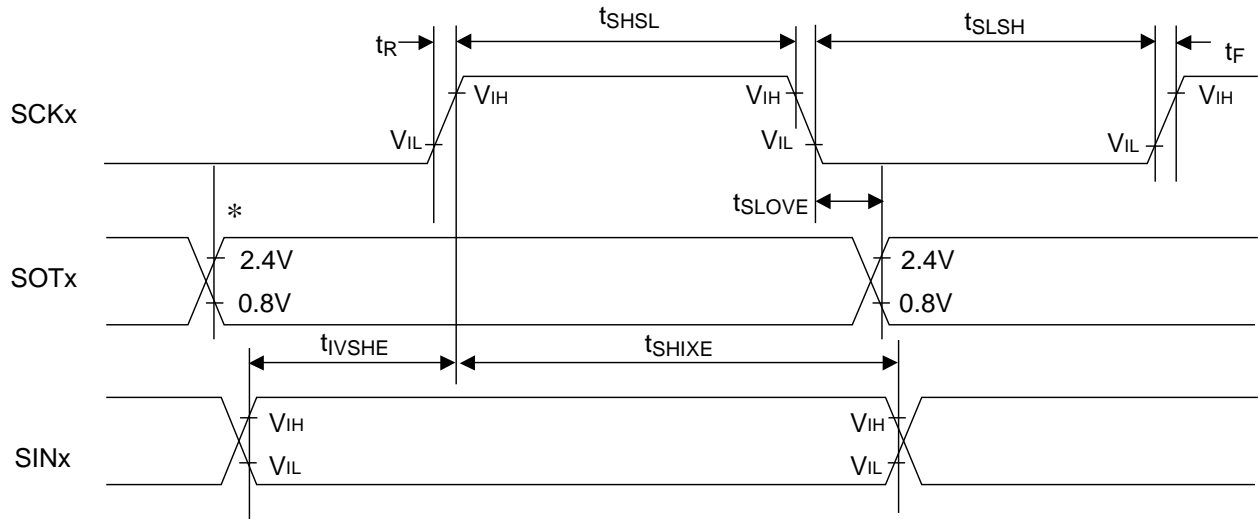
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters. Refer to Hardware Manual for details.

• Internal shift clock mode



• External shift clock mode

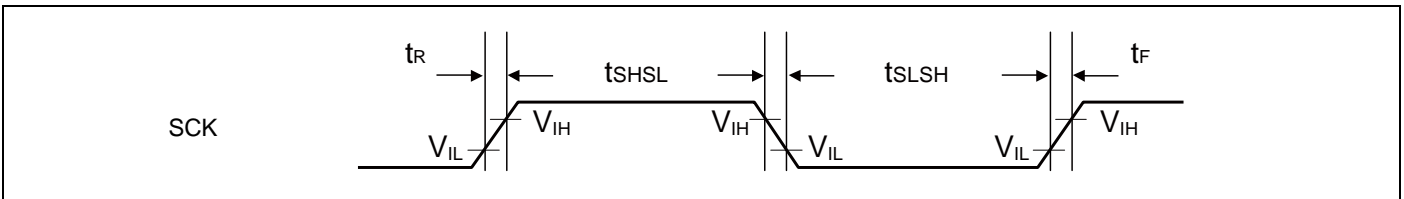


*: Changes when writing to TDR register

13.4.5.2 External Clock (EXT = 1): asynchronous only

(T_A: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC6} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock "H" pulse width	t _{SHSL}	SCK0, SCK1, SCK8, SCK9	C _L =50 pF (When drive capability is 2 mA or more.) C _L =20 pF (When drive capability is 1 mA)	t _{CPP} +10	-	ns
Serial clock "L" pulse width	t _{SLSH}			t _{CPP} +10	-	ns
SCK fall time	t _F			-	5	ns
SCK rise time	t _R			-	5	ns



13.4.5.3 I²C Timing

 (T_A: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Standard mode		High-speed mode		Unit	Remarks	
				Min	Max	Min	Max			
SCL clock frequency	f _{SCL}	SCK0_0, SCK1_0		0	100	0	400	kHz		
Repeat "start" condition hold time SDA ↓→ SCL ↓	t _{HDSTA}	SOT0_0, SOT1_0 (SDA) SCK0_0, SCK1_0 (SCL)		4.0	–	0.6	–	μs		
Width of "L" for SCL clock	t _{LOW}	SCK0_0, SCK1_0 (SCL)		4.7	–	1.3	–	μs		
Width of "H" for SCL clock	t _{HIGH}	SCK0_0, SCK1_0 (SCL)		4.0	–	0.6	–	μs		
Repeat "start" condition setup time SCL ↑→ SDA ↓	t _{SUSTA}	SCK0_0, SCK1_0 (SCL)	C _L = 50 pF (When drive capability is 2 mA or more.) C _L = 20 pF (When drive capability is 1 mA) R = (V _P /I _{OL}) *1	4.7	–	0.6	–	μs		
Data hold time SCL ↓→ SDA ↓↑	t _{HDDAT}	SOT0_0, SOT1_0 (SDA) SCK0_0, SCK1_0 (SCL)		0	3.45 ^{*2}	0	0.9	μs		
Data setup time SDA ↓↑→ SCL ↑	t _{SUDAT}	SOT0_0, SOT1_0 (SDA) SCK0_0, SCK1_0 (SCL)		250 ^{*3}	–	100	–	ns		
"Stop" condition setup time SCL ↑→SDA ↑	t _{SUSTO}	SOT0_0, SOT1_0 (SDA) SCK0_0, SCK1_0 (SCL)		4.0	–	0.6	–	μs		
Bus-free time between "stop" condition and "start" condition	t _{BUF}	–		4.7	–	1.3	–	μs		
Noise filter	t _{SP}	–		–	2t _{CPP} ^{*4}	–	2t _{CPP} ^{*4}	–	ns	

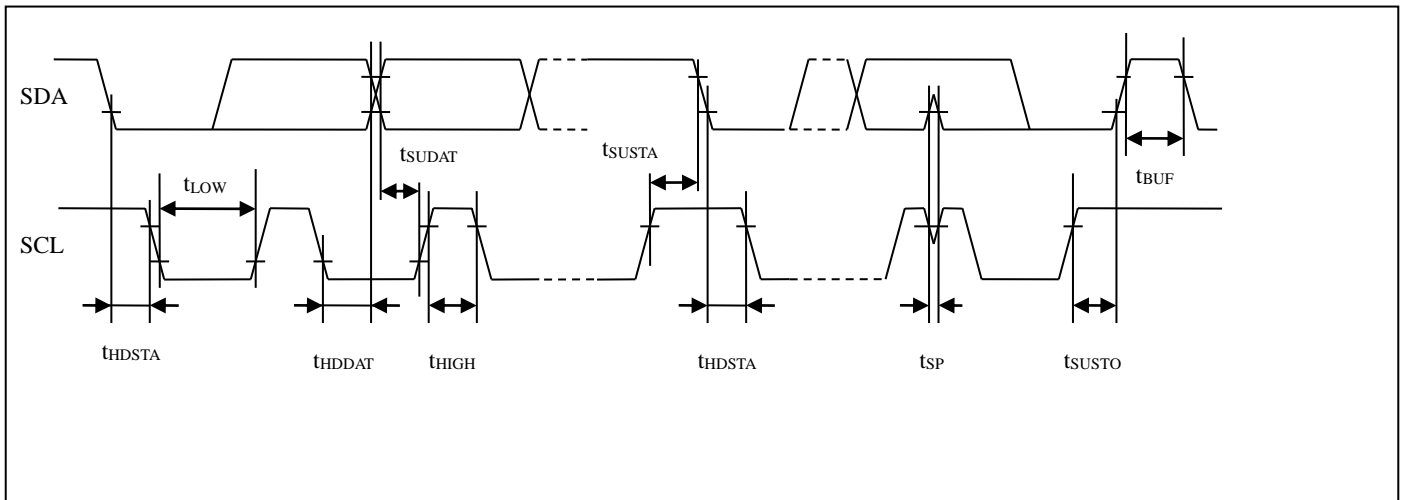
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.

V_P shows the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the peripheral bus clock to 8MHz or more when use I²C.



13.4.6 LIN-UART Timing

Bit setting: ESCR: SCES = 0, ECCR: SCDE = 0

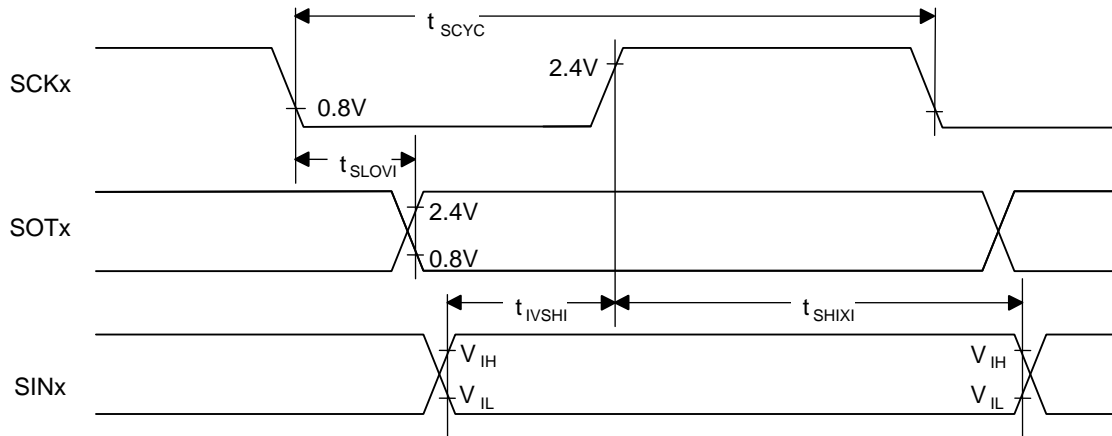
(T_A: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC E} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	-	5t _{CPP}	-	ns	Internal shift clock mode: C _L =80 pF+1 • TTL
SCK ↓ → SOT delay time	t _{SLOVI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		-50	+50	ns	
Valid SIN → SCK ↑ setup time	t _{IVSHI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7,		t _{CPP} +80	-	ns	
SCK ↑ → Valid SIN hold time	t _{SHIXI}	SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		0	-	ns	
Serial clock "L" pulse width	t _{SLSH}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	-	3t _{CPP} -t _R	-	ns	External shift clock mode: C _L =80 pF+1 • TTL
Serial clock "H" pulse width	t _{SHSL}			t _{CPP} +10	-	ns	
SCK ↓ → SOT delay time	t _{SLOVE}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		-	2t _{CPP} +60	ns	
Valid SIN → SCK ↑ setup time	t _{IVSHE}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7,		30	-	ns	
SCK ↑ → Valid SIN hold time	t _{SHIXE}	SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		t _{CPP} +30	-	ns	
SCK fall time	t _F	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7		-	10	ns	
SCK rise time	t _R			-	40	ns	

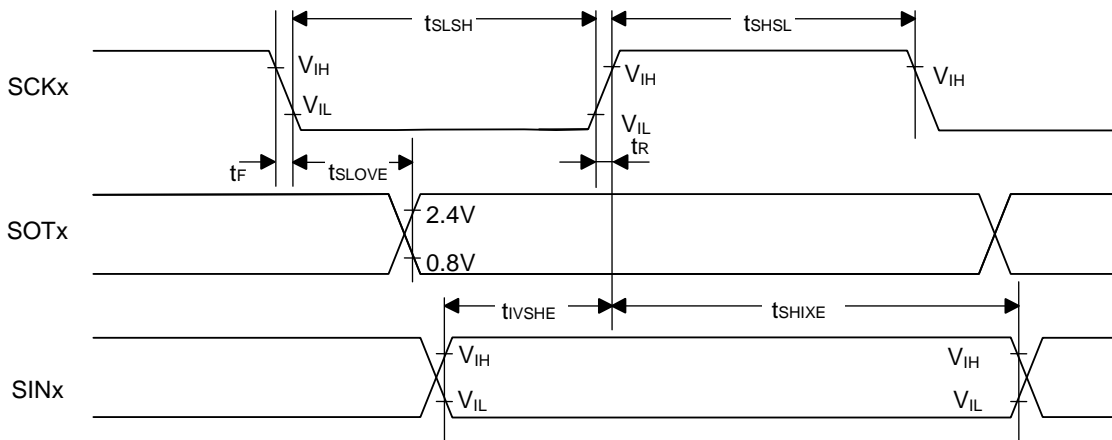
Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. Refer to Hardware Manual for details.

Internal Shift Clock Mode



External Shift Clock Mode



Bit setting: ESCR: SCES=1, ECCR: SCDE=0

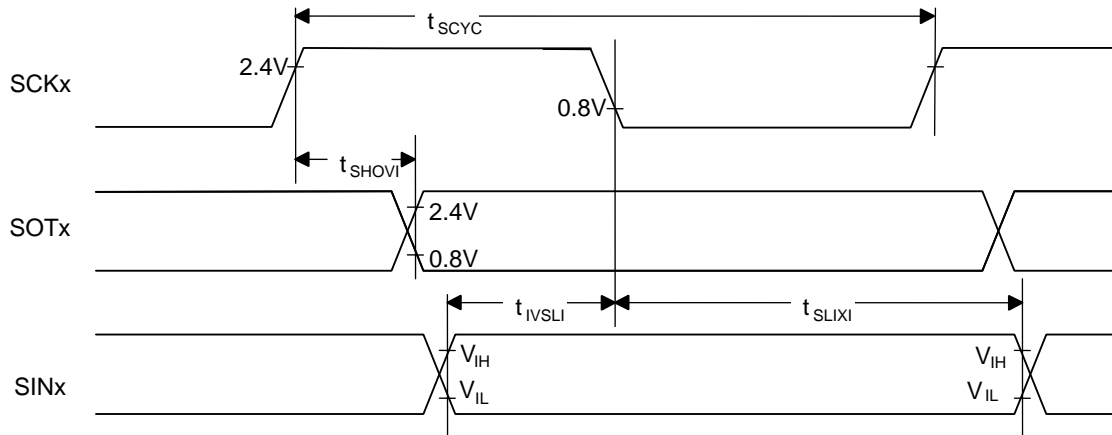
(TA: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC E} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	-	5t _{CPP}	-	ns	Internal shift clock mode: C _L =80 pF+1 • TTL
SCK ↑→ SOT delay time	t _{SHOVI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		-50	+50	ns	
Valid SIN→ SCK ↓setup time	t _{IVSLI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		t _{CPP} +80	-	ns	
SCK ↓→ Valid SIN hold time	t _{SLIXI}			0	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	-	3t _{CPP} -t _R	-	ns	External shift clock mode: C _L =80 pF+1 • TTL
Serial clock "L" pulse width	t _{SLSH}			t _{CPP} +10	-	ns	
SCK ↑→ SOT delay time	t _{SHOVE}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		-	2t _{CPP} +60	ns	
Valid SIN → SCK ↓setup time	t _{IVSLE}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		30	-	ns	
SCK ↓→ Valid SIN hold time	t _{SLIXE}			t _{CPP} +30	-	ns	
SCK fall time	t _F	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7		-	10	ns	
SCK rise time	t _R			-	40	ns	

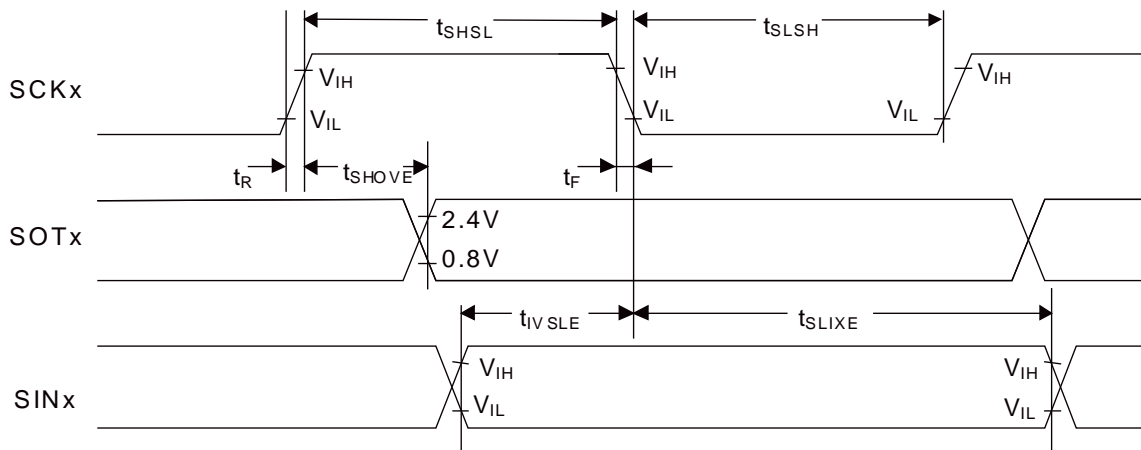
Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. Refer to Hardware Manual for details.

Internal Shift Clock Mode



External Shift Clock Mode



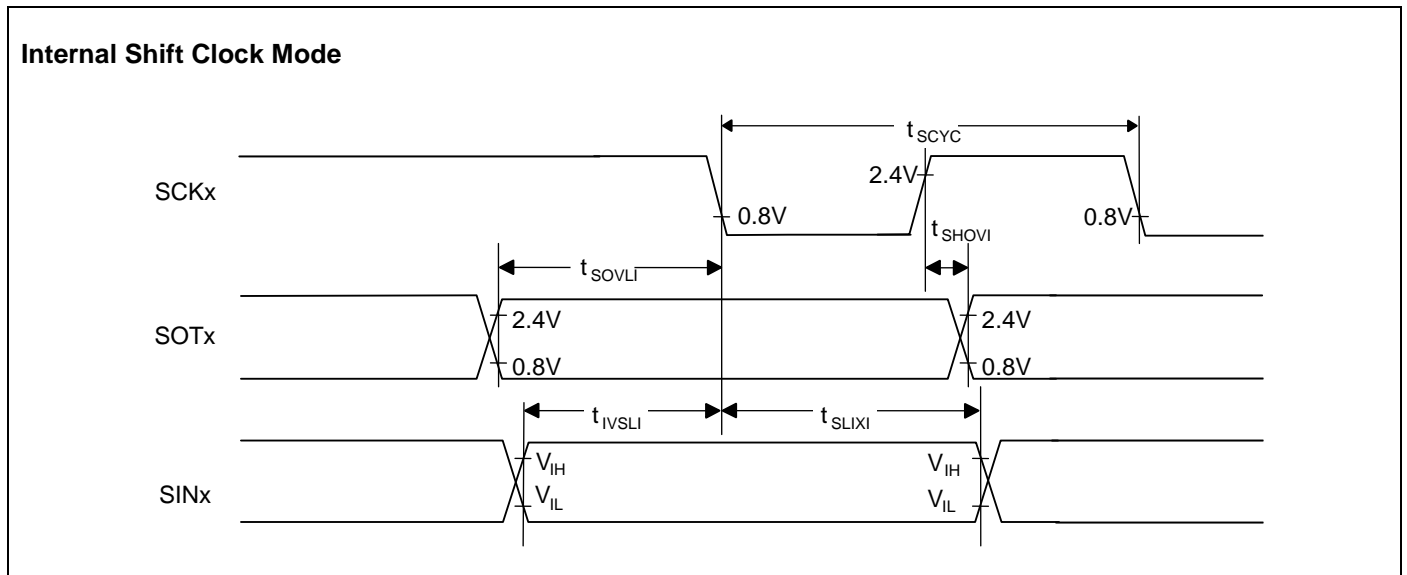
Bit setting: ESCR: SCES = 0, ECCR: SCDE = 1

(TA: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC6} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	-	5t _{CPP}	-	ns	Internal shift clock mode: C _L =80 pF+1 • TTL
SCK ↑→ SOT delay time	t _{SHOVI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		-50	+50	ns	
Valid SIN → SCK ↓setup time	t _{IVSLI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7,		t _{CPP} +80	-	ns	
SCK ↓→ Valid SIN hold time	t _{SLIXI}	SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		0	-	ns	
SOT → SCK ↓ delay time	t _{SOVLI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		3t _{CPP} -70	-	ns	

Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. Refer to Hardware Manual for details.



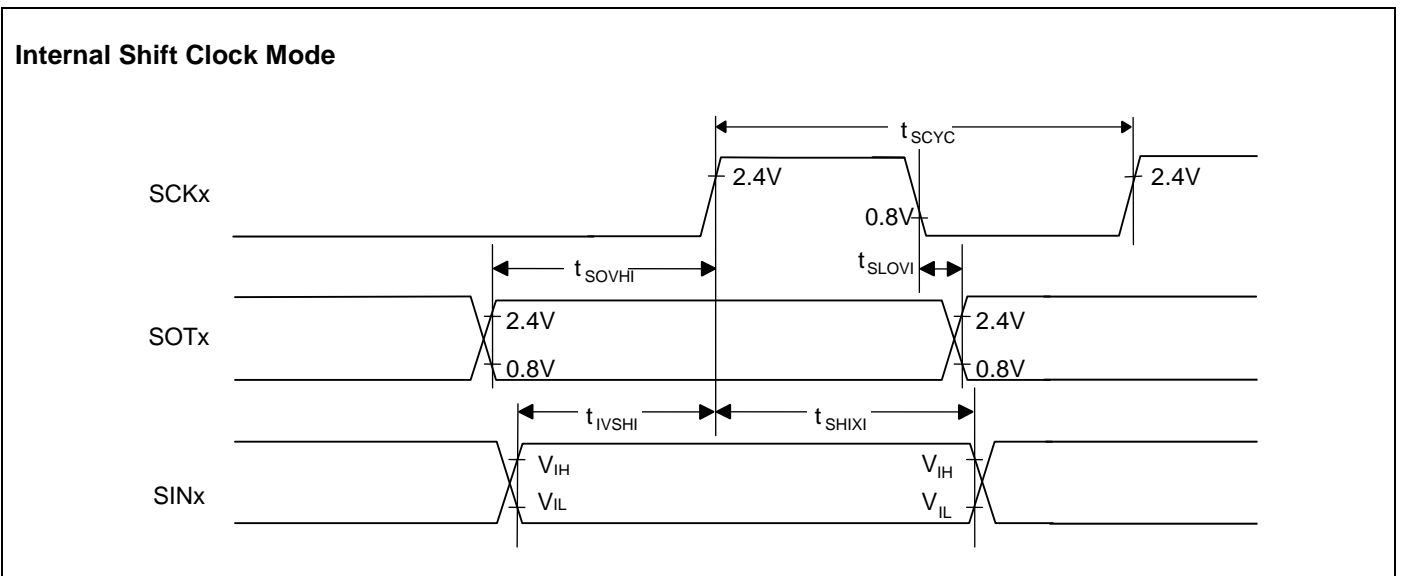
Bit setting: ESCR: SCES = 1, ECCR: SCDE = 1

(TA: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC E} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	-	5t _{CPP}	-	ns	Internal shift clock Mode: C _L =80 pF+1 • TTL
SCK ↓→ SOT delay time	t _{SLOVI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		-50	+50	ns	
Valid SIN→ SCK ↑ setup time	t _{IVSHI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7		t _{CPP} +80	-	ns	
SCK ↑→ Valid SIN hold time	t _{SHIXI}	SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		0	-	ns	
SOT → SCK ↑ delay time	t _{SOVHI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		3t _{CPP} -70	-	ns	

Notes:

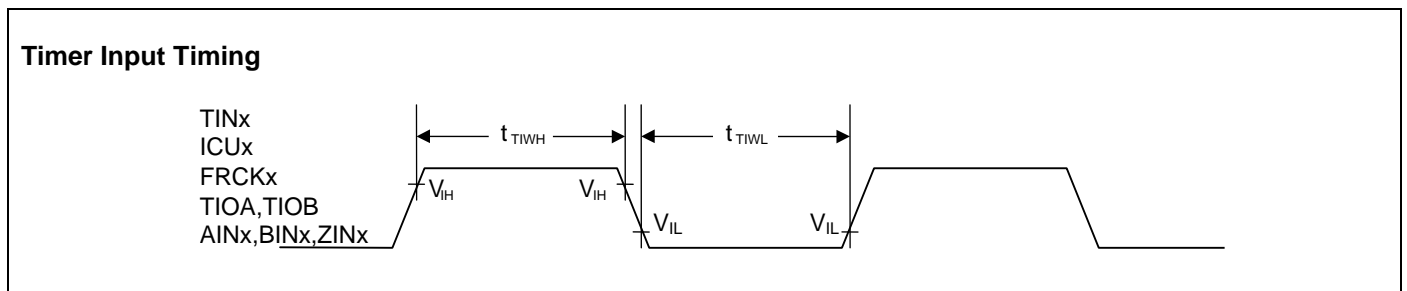
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. Refer to Hardware Manual for details.



13.4.7 Timer Input Timing

(T_A: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC E} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

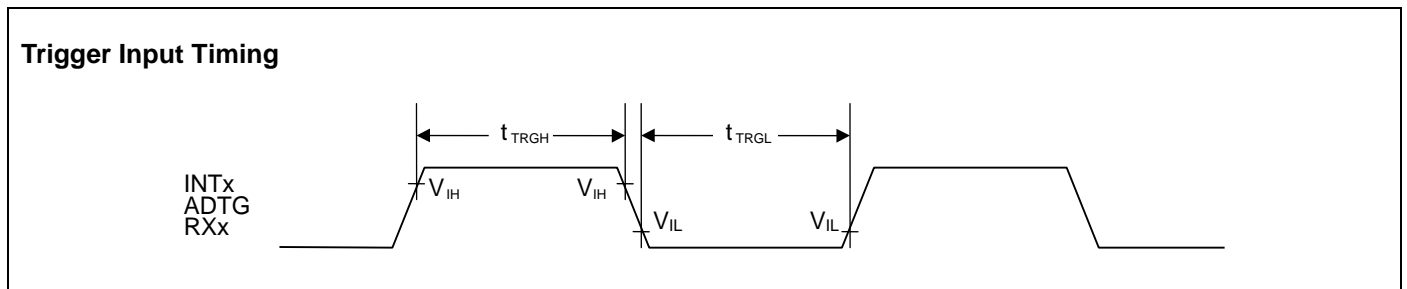
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t _{TIWH} , t _{TIWL}	TIN0, TIN1, TIN2, TIN3, ICU0 to ICU11, FRCK0 to FRCK5, TIOA, TIOB, AIN0, BIN0, ZIN0 , AIN1, BIN1, ZIN1	–	4t _{CPP}	–	ns



13.4.8 Trigger input timing

(T_A: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{CC E} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

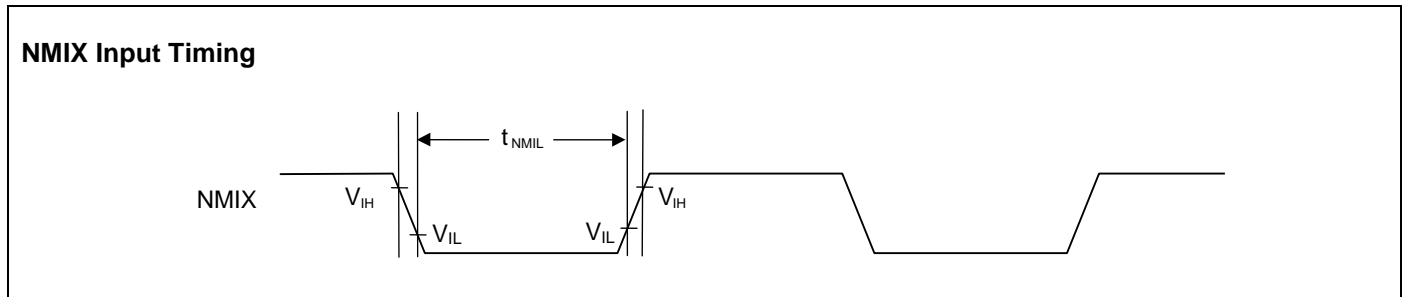
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{TRGH} , t _{TRGL}	INT0 to INT15, ADTG, RX0 to RX2	–	5t _{CPP}	–	ns	
				1	–	µs	In stop mode



13.4.9 NMI Input Timing

(TA: Recommended operating conditions, V_{CC5} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t _{NMIL}	NMIX	–	4t _{CPP}	–	ns



13.4.10 Low Voltage Detection (External Low-voltage Detection)

(TA: Recommended operating conditions, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V _{CC5}	V _{CC5}	–	–	–	5.5	V	
Detection voltage	V _{DL}	V _{CC5}	*1	3.9	4.1	4.3	V	When power-supply voltage falls and detection level is set initially
Hysteresis width	V _{HYS}	V _{CC5}	–	–	–	125	mV	When power-supply voltage rises
Low voltage detection time	T _d	–	–	–	–	30	µs	
Power supply voltage fluctuation rate	–	V _{CC5}	–	-2	–	2	V/ms	*2

*1: If the power supply voltage fluctuates within the time less than the low-voltage detection time (T_d), there is a possibility that the low-voltage detection will occur or stop after the power supply voltage passes the detection range.

*2: In order to perform the low-voltage detection at the detection voltage (V_{DL}), be sure to suppress fluctuation of the power supply voltage within the limits of the power supply voltage fluctuation rate.

13.4.11 Low Voltage Detection (Internal Low-voltage Detection)

(TA: Recommended operating conditions, VSS = AVSS = 0.0V)

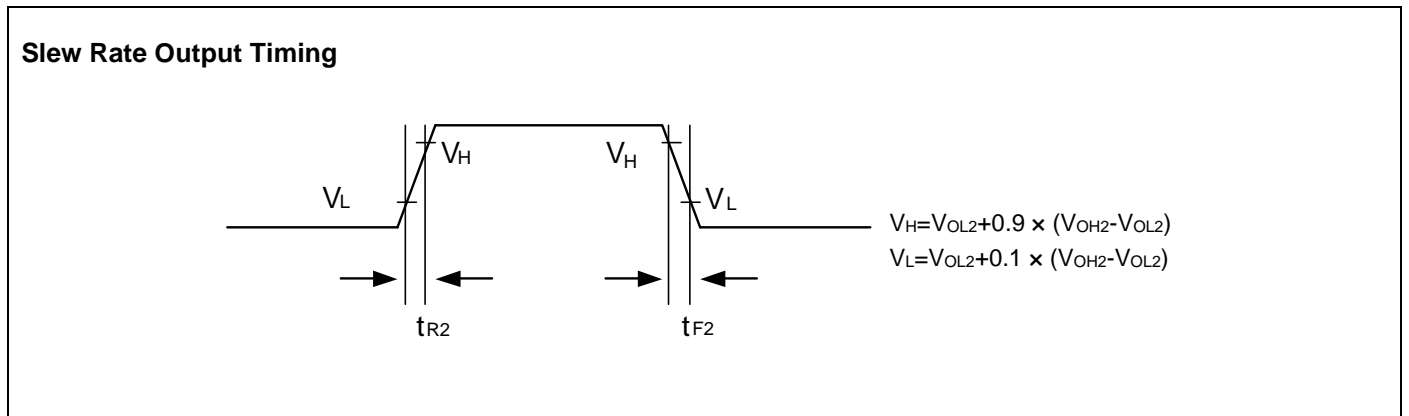
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V _{RDP5}	V _{CC}	—	—	—	1.3	V	
Detection voltage	V _{RDL}		*	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V _{RHYS}		—	—	—	50	mV	When power-supply voltage rises
Low voltage detection time	T _d	—	—	—	—	30	μs	

*: If the fluctuation of the power supply is faster than the low voltage detection time (T_d), there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

13.4.12 High Current Output Slew Rate

(TA: Recommended operating conditions, DV_{CC5} = AV_{CC} = 5.0V±10%, VSS = AVSS = 0.0V)

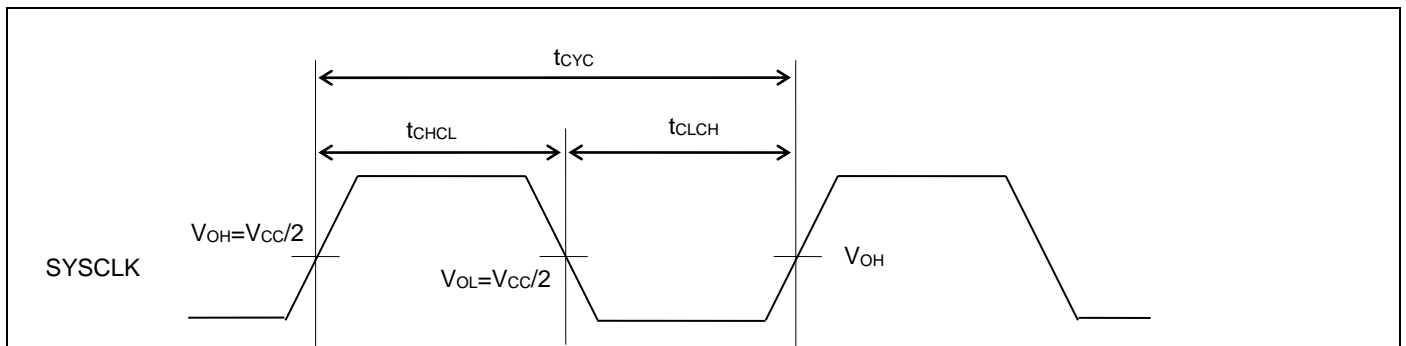
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise /fall time	t _{R2} , t _{F2}	P060 to P067, P070 to P077, P080 to P087	—	15	—	100	ns	load capacitance 85 pF



13.4.13 Clock Output Timing

(TA: Recommended operating conditions, $V_{CC5} = V_{CCE} = AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	SYSCLK	—	t_{CPT}	—	ns	
SYSCLK $\uparrow \rightarrow$ SYSCLK \downarrow	t_{CHCL}	SYSCLK		$(1/2 t_{CYC}) - 7$	$(1/2 t_{CYC}) + 7$	ns	
SYSCLK $\downarrow \rightarrow$ SYSCLK \uparrow	t_{CLCH}	SYSCLK		$(1/2 t_{CYC}) - 7$	$(1/2 t_{CYC}) + 7$	ns	



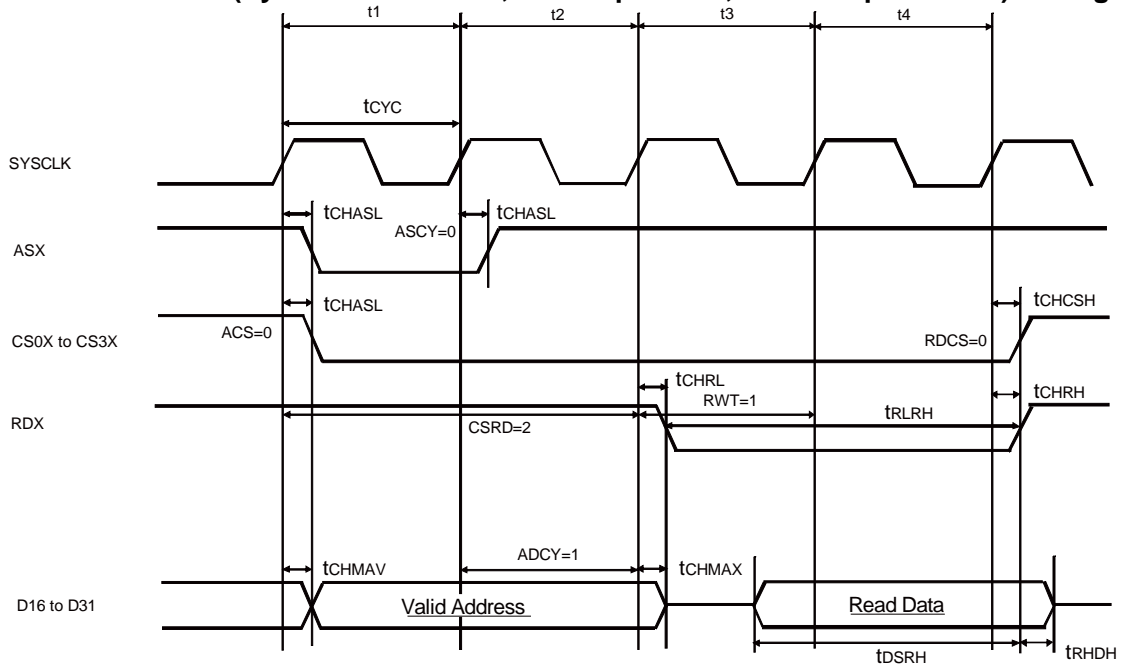
13.4.14 External Bus I/F (Synchronous Mode) Timing

(T_A: Recommended operating conditions, V_{CC5} = V_{CCE} = AV_{CC} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)
(External load capacitance 50pF)

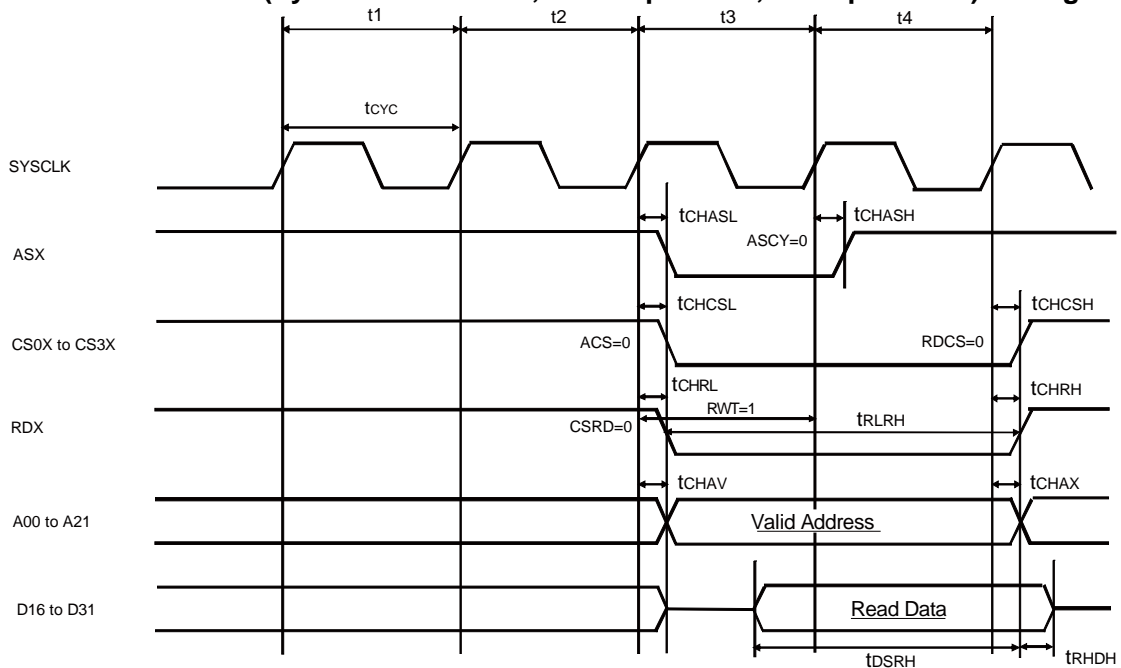
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Cycle time	t _{CYC}	SYSCLK	25	–	ns	
ASX delay time	t _{CHASL} , t _{CHASH}	SYSCLK, ASX	0.5	18	ns	
CS0X to CS3X delay time	t _{CHCSL} , t _{CHCSH}	SYSCLK, CS0X to CS3X	0.5	18	ns	
A00 to A21 delay time	t _{CHAV} , t _{CHAX}	SYSCLK, A00 to A21	0.5	18	ns	
RDX delay time	t _{CHRL} , t _{CHRH}	SYSCLK, RDX	0.5	18	ns	
RDX minimum pulse	t _{RLRH}	RDX	t _{CYC} × 2 - 20	–	ns	RWT=1, set RWT to 1 or more. *
Data setup → RDX ↑ time	t _{DSRH}	RDX, D16 to D31	18 + t _{CYC}	–	ns	RWT=1, set RWT to 1 or more. *
RDX ↑ → data hold	t _{RHDH}		0	–	ns	
WRnX delay time	t _{CHWL} , t _{CHWH}	SYSCLK, WR0X, WR1X	0.5	18	ns	
WRnX minimum pulse width	t _{WLWH}	WR0X, WR1X	t _{CYC} - 10	–	ns	WWT=0 *
SYSCLK ↑ → data output time	t _{CHDV}	SYSCLK, D16 to D31	0.5	18	ns	
SYSCLK ↑ → data hold time	t _{CHDX}		–	18	ns	Set WRCS to 1 or more.
SYSCLK ↑ → address output time	t _{CHMAV}		0.5	18	ns	
SYSCLK ↑ → address hold time	t _{CHMAX}	SYSCLK, D16 to D31	–	18	ns	In multiplex mode, set as follows: Set CSWR and CSRD to 2 or more. ASCY must satisfy the following conditions because of setting ADCY>ASCY and protocol violation prevention. ADCY + 1 ≤ ACS + CSRD ADCY + 1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR Refer to Hardware Manual for details.

*: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

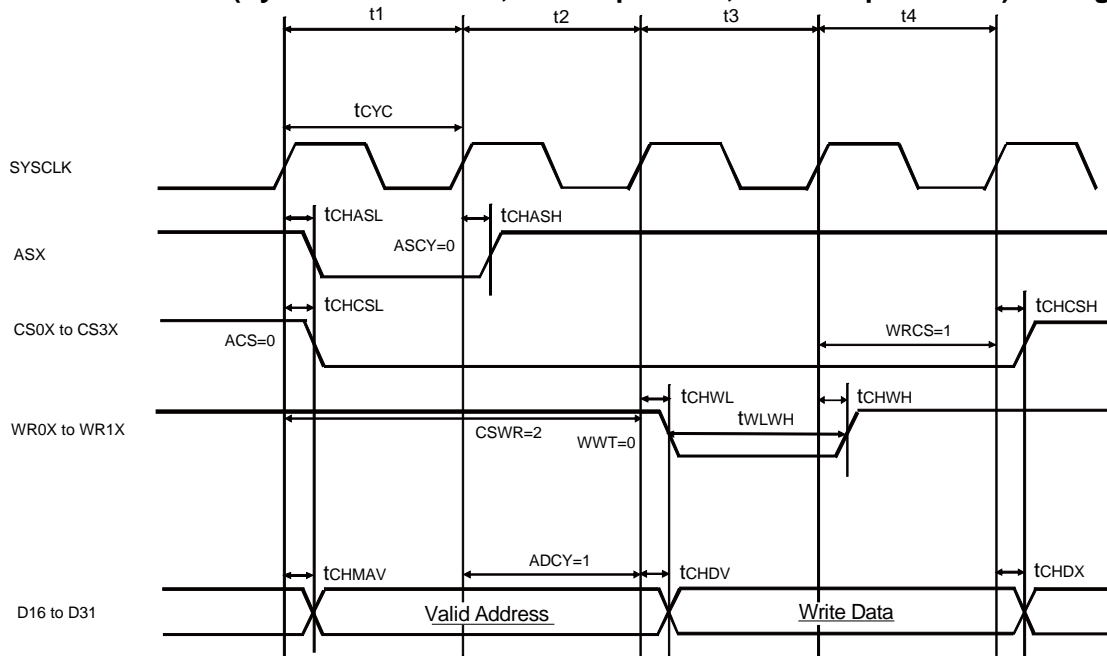
External Bus I/F (Synchronous Mode, Read Operation, and Multiplex Mode) Timing



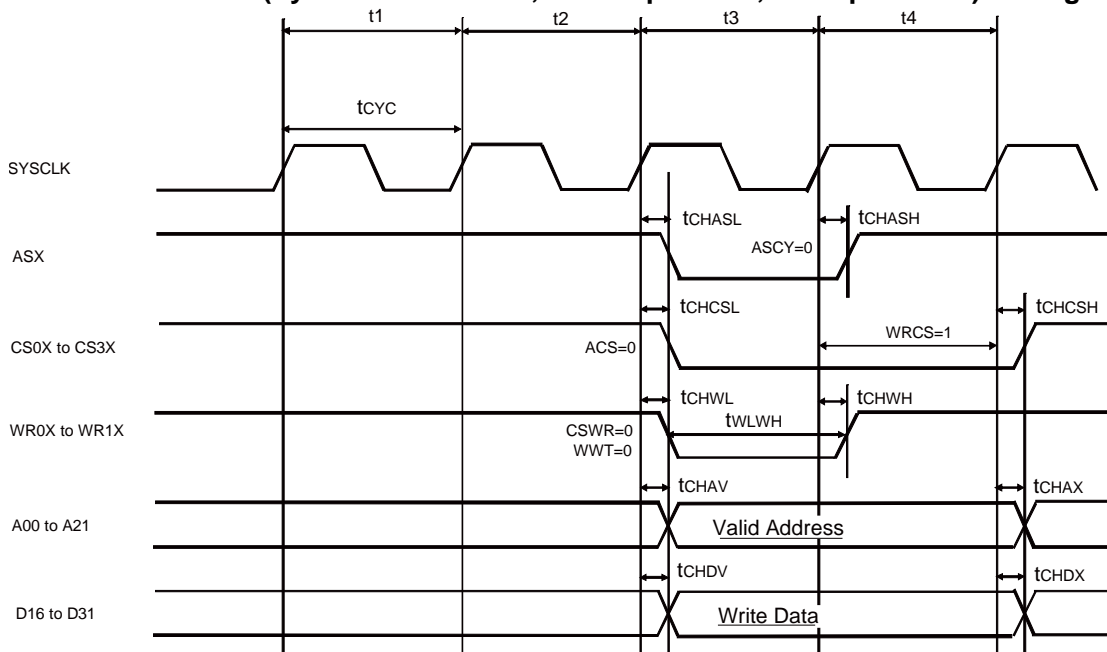
External Bus I/F (Synchronous Mode, Read Operation, and Split Mode) Timing



External Bus I/F (Synchronous Mode, Write Operation, and Multiplex Mode) Timing



External Bus I/F (Synchronous Mode, Write Operation, and Split Mode) Timing



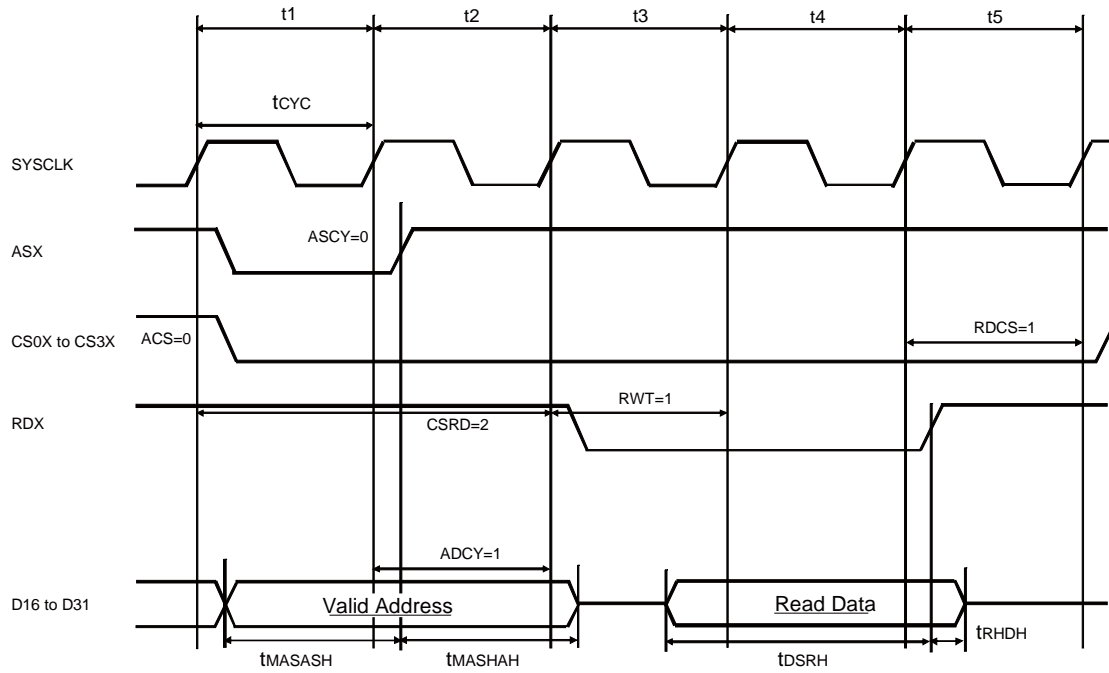
13.4.15 External Bus I/F (Asynchronous Mode) Timing

(TA: Recommended operating conditions, $V_{CC5} = V_{CC E} = AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0V$)
(External load capacitance 50pF)

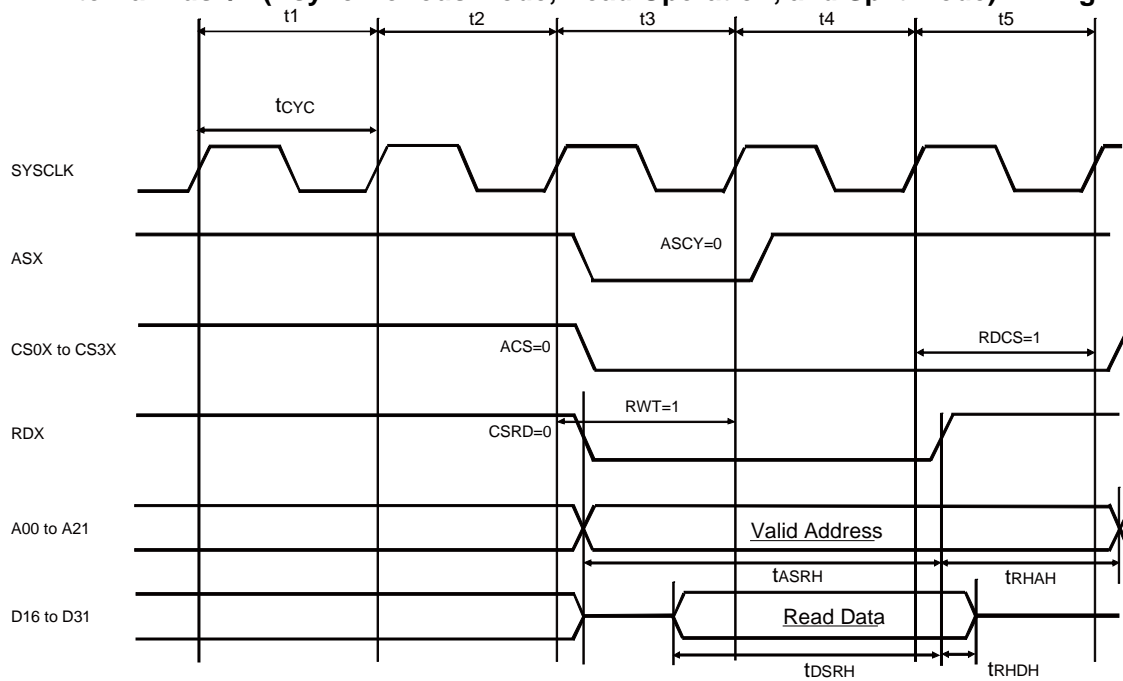
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	–	ns	
Address setup → RDX↑time	t_{ASRH}	RDX, A00 to A21	$2 \times t_{CYC} - 12$	$2 \times t_{CYC} + 12$	ns	RWT=1, Set RWT to “1” or more. *
RDX ↑→ Address hold	t_{RHAH}		$t_{CYC} - 12$	$t_{CYC} + 12$	ns	Set RDCS to “1” or more.
Data setup → RDX↑time	t_{DSRH}	RDX, D16 to D31	$18 + t_{CYC}$	–	ns	RWT=1, Set RWT to “1” or more.
RDX ↑ → Data hold	t_{RHDH}		0	–	ns	
Address setup → WRnX↑time	t_{ASWH}	WR0X to WR1X, A00 to A21	$t_{CYC} - 12$	$t_{CYC} + 12$	ns	WWT=0 *
WRnX ↑→ Address hold	t_{WHAH}		$t_{CYC} - 12$	$t_{CYC} + 12$	ns	Set WRCS to “1” or more.
Data setup → WRnX ↑ time	t_{DSWH}	WR0X to WR1X, D16 to D31	$t_{CYC} - 16$	$t_{CYC} + 16$	ns	WWT=0 *
WRnX ↑→ Data hold	t_{WHDH}		$t_{CYC} - 16$	$t_{CYC} + 16$	ns	Set WRCS to “1” or more.
Address setup → ASX↑time	t_{MASASH}	ASX, D16 to D31	$t_{CYC} - 16$	$t_{CYC} + 16$	ns	ASCY=0
ASX ↑→ Address hold	t_{MASHAH}		$t_{CYC} - 16$	$t_{CYC} + 16$	ns	In multiplex mode, set as follows: Set CSWR and CSRD to 2 or more. ASCY must satisfy the following conditions because of setting ADCY>ASCY and protocol violation prevention. $ADCY + 1 \leq ACS + CSRD$ $ADCY + 1 \leq ACS + CSWR$ $ASCY + 1 \leq ACS + CSRD$ $ASCY + 1 \leq ACS + CSWR$ Refer to Hardware Manual for details.

*: If the bus is expanded by automatic wait insertion or RDY input, add time ($t_{CYC} \times$ the number of expanded cycles) to the rated value.

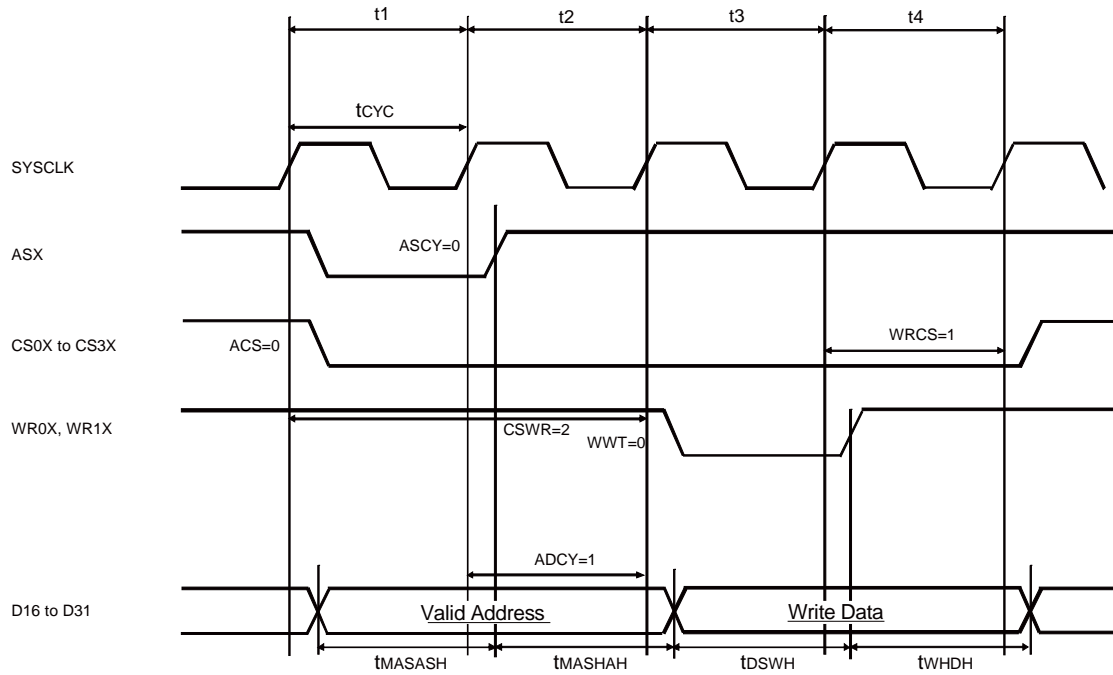
External Bus I/F (Asynchronous Mode, Read Operation, and Multiplex Mode) Timing



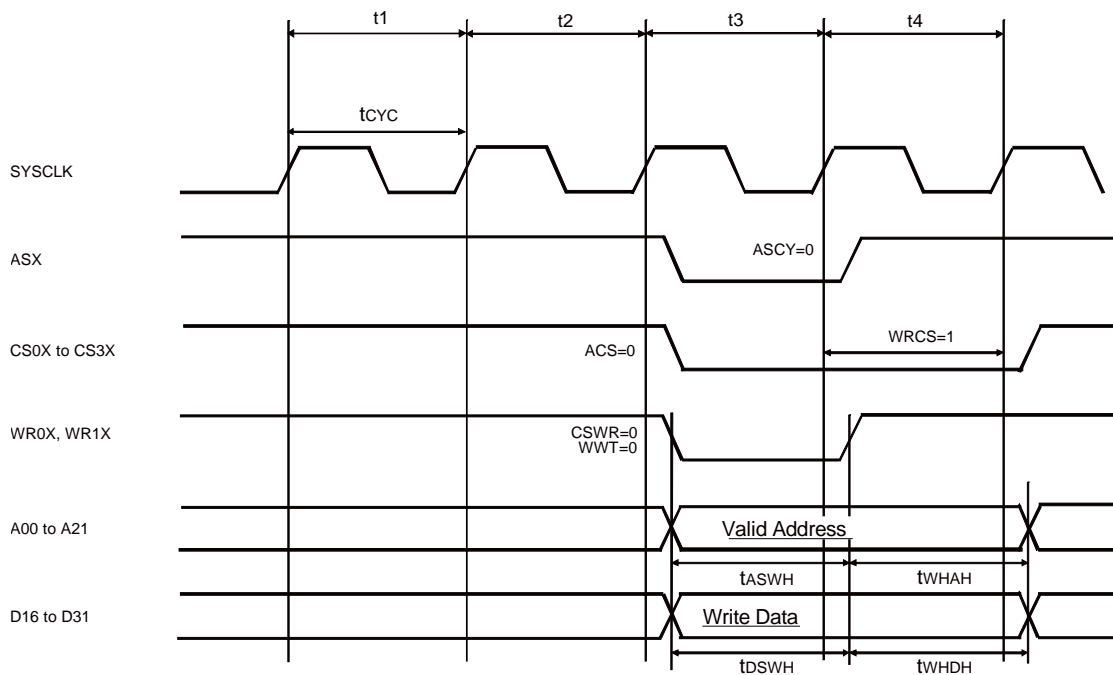
External Bus I/F (Asynchronous Mode, Read Operation, and Split Mode) Timing



External Bus I/F (Asynchronous Mode, Write Operation, and Multiplex Mode) Timing



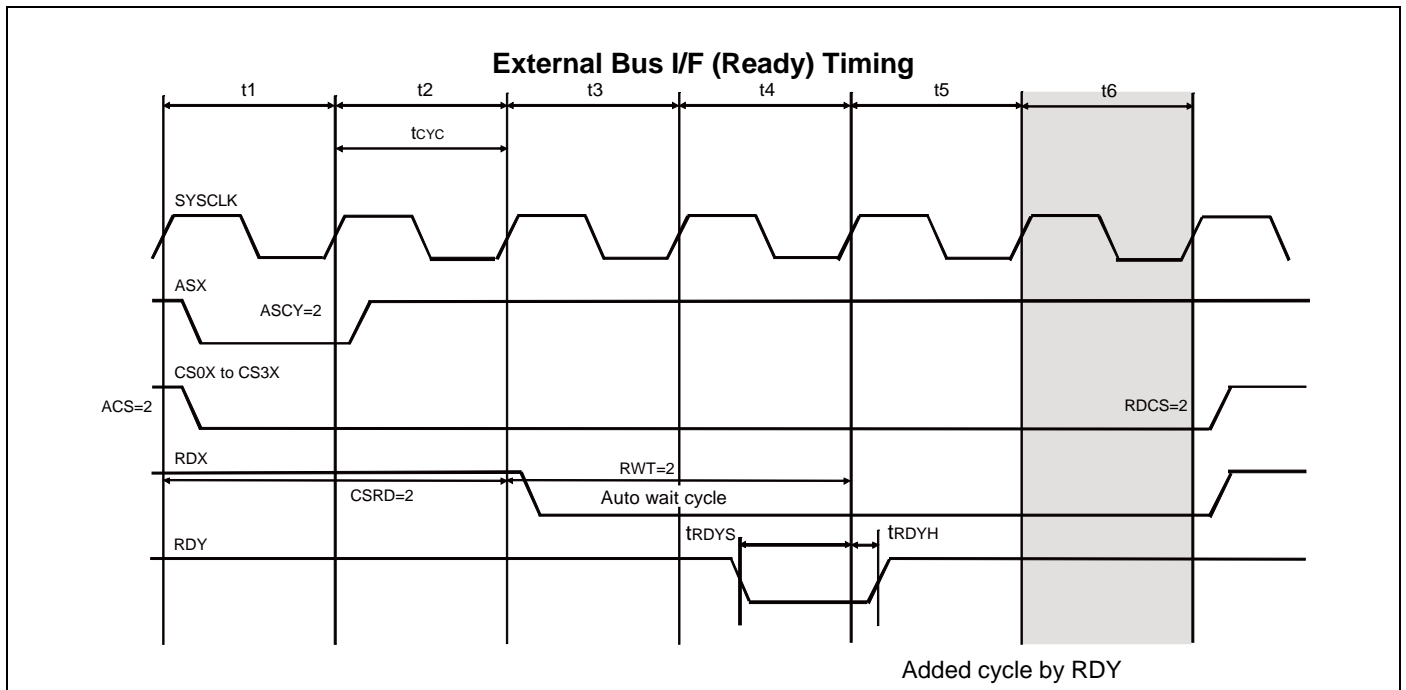
External Bus I/F (Asynchronous Mode, Write Operation, and Split Mode) Timing



13.4.16 External Bus I/F (Ready) Timing

(TA: Recommended operating conditions, $V_{cc5} = V_{ccE} = AV_{cc} = 5.0V \pm 10\%$, $V_{ss} = AV_{ss} = 0.0V$)
 (External load capacitance 50pF)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{cyc}	SYSCLK	50	–	ns	If using RDY, set SYSCLK to 20 MHz or less.
RDY setup time → SYSCLK ↑	t_{RDYS}	SYSCLK, RDY	28	–	ns	
SYSCLK ↑ → RDY hold time	t_{RDYH}	SYSCLK, RDY	0	–	ns	



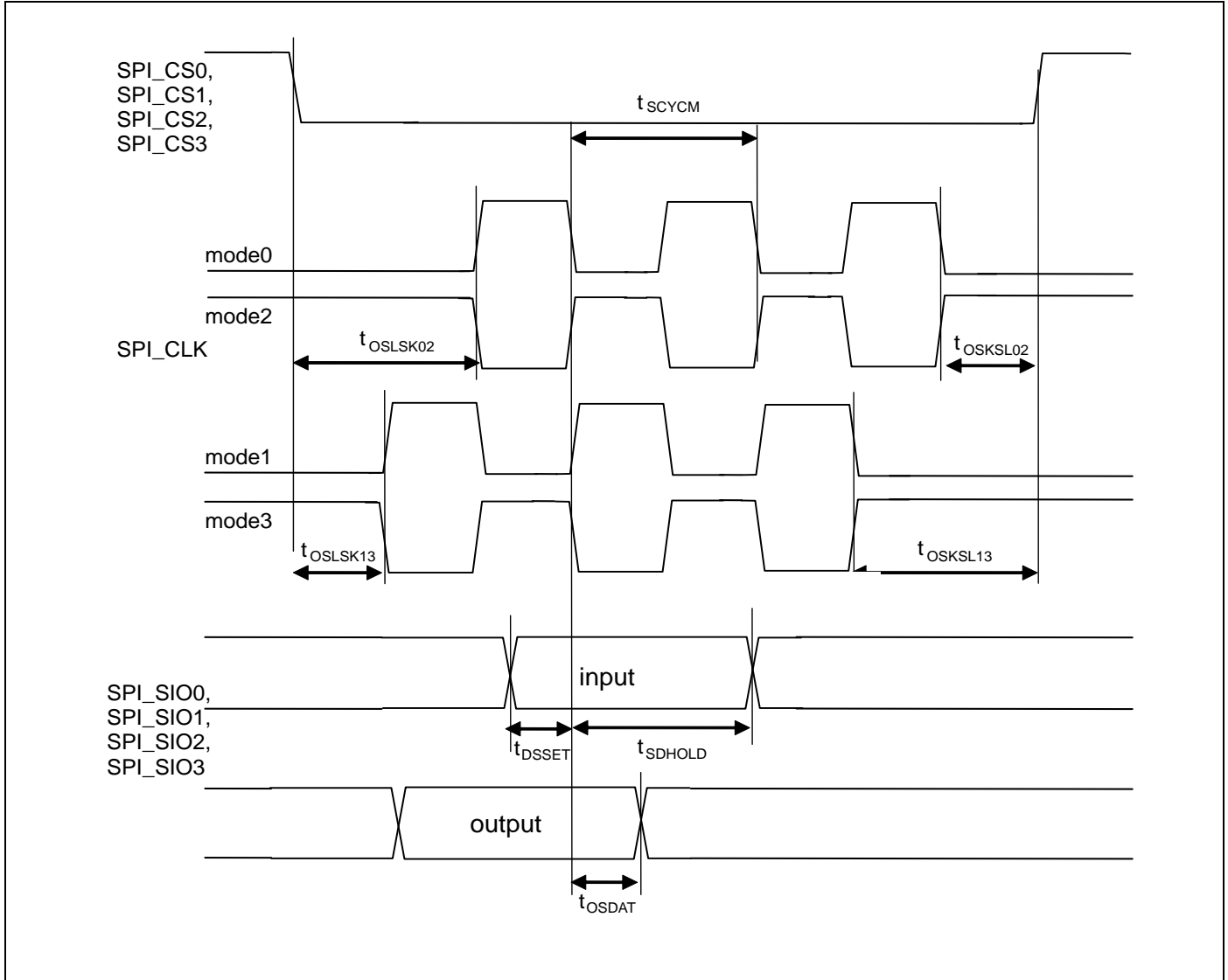
13.4.17 HS-SPI Timing

(TA: Recommended operating conditions, $V_{CC5} = V_{CC E} = AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0V$)
 (External load capacitance 20pF)

Parameter	Symbol	Pin Name	Condi tions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYCM}	SPI_CLK	Master	62.5	—	ns	*1 *2
			Slave	100	—	ns	
Valid CS → CLK start time (mode0/mode2)	$t_{OSLSK02}$	SPI_CLK, SPI_CS0, SPI_CS1, SPI_CS2, SPI_CS3	—	$1.5 \times t_{SCYCM} - 15$	—	ns	
Valid CS → CLK start time (mode1/mode3)	$t_{OSLSK13}$			$t_{SCYCM} - 15$	—	ns	
CLK end → Invalid CS time (mode0/mode2)	$t_{OSKSL02}$			$t_{SCYCM} - 10$	—	ns	
CLK end → Invalid CS time (mode1/mode3)	$t_{OSKSL13}$			$1.5 \times t_{SCYCM} - 10$	—	ns	
SIO data output time	t_{OSDAT}	SPI_CLK, SPI_SIO0, SPI_SIO1, SPI_SIO2, SPI_SIO3	Master	-10	15	ns	
			Slave	—	28	ns	
SIO setup	t_{DSSET}	SPI_CLK, SPI_SIO0, SPI_SIO1, SPI_SIO2, SPI_SIO3	—	22	—	ns	
SIO hold	t_{SDHOLD}			$0.5 \times t_{SCYCM}$	—	ns	

*1: $V_{CC E} = 5.0 V \pm 10\%$, or $V_{CC E} = 3.0$ to $3.6 V$

*2: In the voltage range shown in *1, this parameter is defined when IOH is -2 mA and IOL is 2 mA.



13.5 A/D Converter
13.5.1 Electrical Characteristics

 (TA: Recommended operating conditions, $V_{CC5} = 5.0V \pm 10\%$, $AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	–	–	± 3.0	LSB	
Non linearity error	–	–	–	–	± 2.5	LSB	
Differential linearity error	–	–	–	–	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN39	AV_{SS} -1.5LSB	–	AV_{SS} +2.5LSB	V	1LSB= ($AV_{CC}-AV_{SS}$) /1024
Full-scale transition voltage	V_{FST}	AN0 to AN39	AV_{CC} -3.5LSB	–	AV_{CC} +0.5LSB	V	
Sampling time	t_{SMP}	–	1.2	–	–	μs	*1
Compare time	t_{CMP}	–	1.8	–	–	μs	*1
A/D conversion time	t_{CNV}	–	3.0	–	–	μs	*1
Analog port input current	I_{AIN}	AN0 to AN39	-5	–	+5	μA	$V_{AVSS} \leq V_{AIN} \leq V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN39	AV_{SS}	–	AVRH	V	
Reference voltage	AVRH	AVRH	4.5	–	5.5	V	$AV_{CC} \geq AVRH$
	AVRL	AV_{SS}	–	0.0	–	V	
Power supply current	I_A	AV_{CC}	–	–	4.0	mA	
	I_{AH}		–	–	6.0	μA	*2
	I_R	AVRH	–	600	900	μA	
	I_{RH}		–	–	5	μA	*2
Variation between channels	–	AN0 to AN39	–	–	4	LSB	

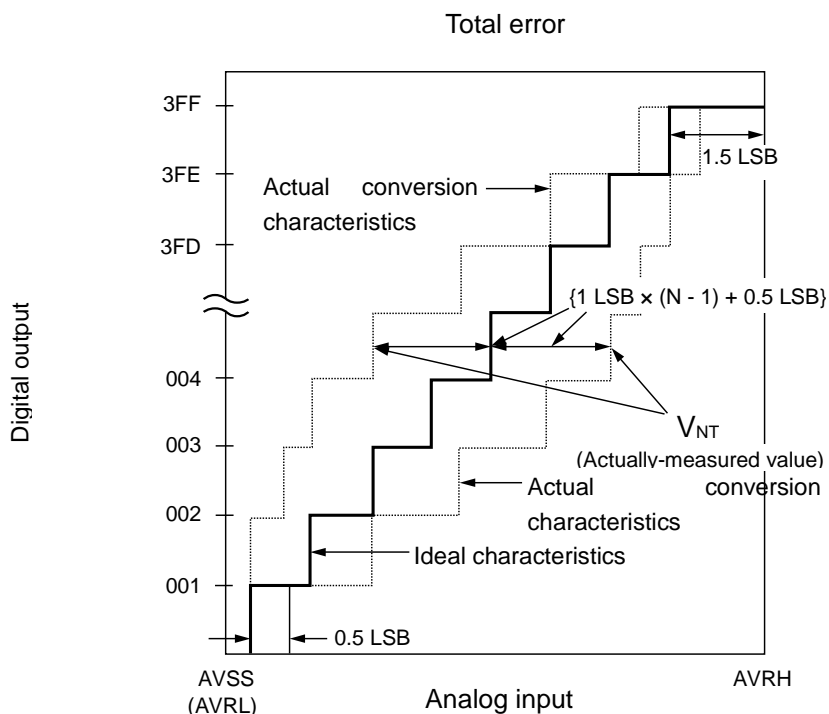
*1: Time for each channel.

 *2: Power supply current ($V_{CC} = AV_{CC} = 5.0 V$) is specified if A/D converter is not operating and CPU is stopped.

Note: Be sure to use the clock with a frequency between 8MHz and 17MHz for the ADC compare clock in order to ensure its accuracy.

13.5.2 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("00 0000 0000" ←→ "00 0000 0001") to the full-scale transition point ("11 1111 1110" ←→ "11 1111 1111").
- Differential linearity error : Deviation of the input voltage from the ideal value that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linearity error.



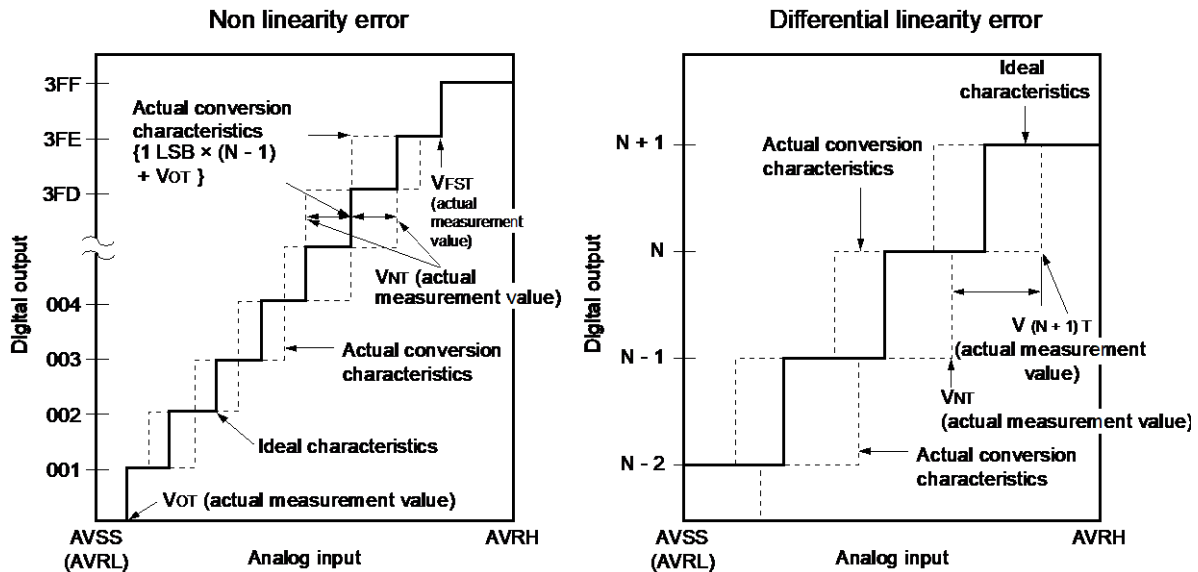
$$\text{Total error of digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + 0.5\text{LSB}\}}{1\text{LSB}} \quad [\text{LSB}]$$

$$1\text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVSS}}{1024} \quad [\text{V}]$$

$$V_{OT} \text{ (Ideal value)} = \text{AVSS} + 0.5 \text{LSB} [\text{V}]$$

$$V_{FST} \text{ (Ideal value)} = \text{AVRH} - 1.5 \text{LSB} [\text{V}]$$

V_{NT} : Voltage at which the digital output changes from (N - 1) to N.



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{OT}\}}{1\text{LSB}} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 \text{LSB [LSB]}$$

$$1\text{LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

V_{OT} : Voltage at which the digital output changes from “000_H” to “001_H”.

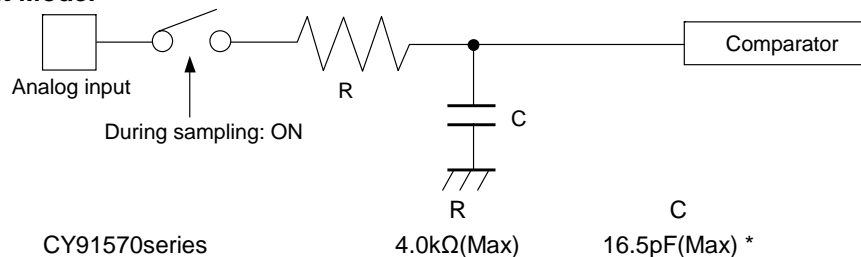
V_{FST} : Voltage at which the digital output changes from “3FE_H” to “3FF_H”.

13.5.3 Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

- External impedance values of the external input of 4.2 kΩ or lower (sampling time = 1.2 μs@ machine clock of 16 MHz) are recommended. When the external impedance is too high, the sampling time for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 μF) to the analog input pin.

Analog Input Circuit Model



Note: Listed values must be considered as reference values.

*: except DA shared pin

13.6 D/A Converter

 (T_A: Recommended operating conditions, V_{CC5} = AV_{CC} = 5.0V±10%, V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	8	bit	
Differential linearity error	—	—	—	—	±3.0	LSB	
Conversion time	—	—	—	0.58	0.69	μs	Load capacitance: 20 pF
	—	—	—	2.90	3.43	μs	Load capacitance: 100 pF
Reference voltage supply current	IDVR	AV _{CC}	—	475	580	μA	Per 1ch *
	IDVRS	AV _{CC}	—	—	7.5	μA	Per 1ch in power down mode
Analog output impedance	—	—	—	3.8	4.5	kΩ	

 *: Reference voltage supply current (V_{CC} = AV_{CC} = 5.0 V) is specified.

13.7 Flash Memory

13.7.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbyte sector* ¹ , excluding internal preprogramming time
	–	300	1100	ms	8 Kbyte sector* ¹ , including internal preprogramming time
	–	400	2000	ms	64 Kbyte sector* ¹ , excluding internal preprogramming time
	–	700	3700	ms	64 Kbyte sector* ¹ , including internal preprogramming time
8-bit writing time	–	9	288	μs	Exclusive of overhead time at system level* ¹
16-bit writing time	–	12	384	μs	Exclusive of overhead time at system level* ¹
ECC writing time	–	9	288	μs	Exclusive of overhead time at system level* ¹
Erase cycle* ² / Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average T _A = +85°C* ³

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

13.7.2 Notes

While the Flash memory is written or erased, shutdown of the external power (V_{CC5}) is prohibited.

In the application system where V_{CC5} might be shut down while writing or erased, be sure to turn the power off by using an external low-voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*¹), hold V_{CC5} at 2.7 V or more within the duration calculated by the following expression:

$$T_d^{*1}[\mu s] + (\text{period of PCLK} [\mu s] \times 257) + 50 [\mu s]$$

*1: See "13.4. AC characteristics, 13.4.10. Low voltage detection (External low-voltage detection)".

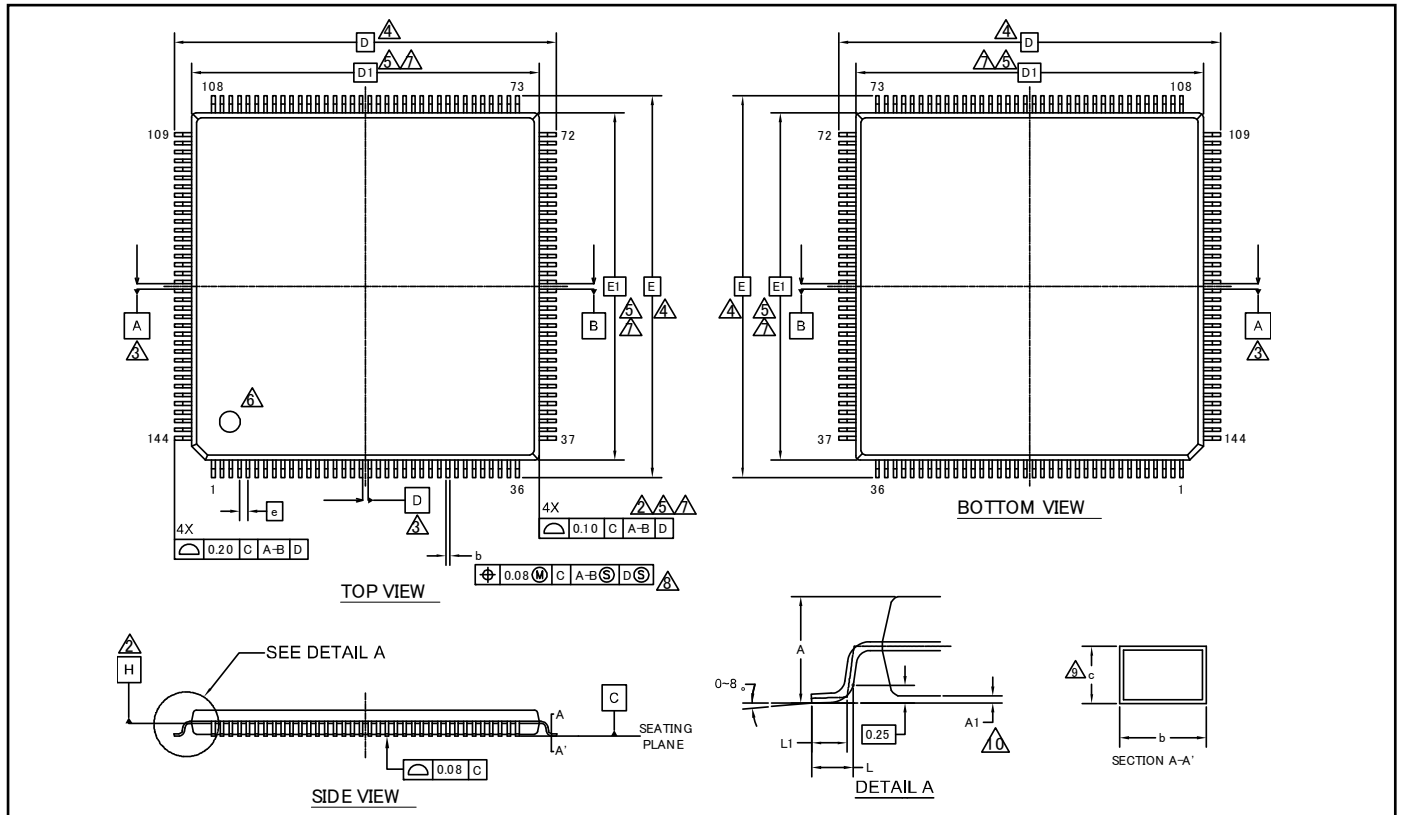
14. Ordering Information

Part Number	Package*
CY91F575BHSPMC-GSE1	LQFP-144 pin, Plastic (LQS144)
CY91F575BPMC-GSE2	
CY91F577BHSPMC-GSE1	
CY91F577BPMC-GSE2	
CY91F579CHSPMC-GSE1	LQFP-144 pin, Plastic (LQN144)
CY91F577BHSPMC1-GSE1	
CY91F579CHSPMC1-GSE1	LQFP-208-pin, Plastic (LQR208)
CY91F579CMPMC-GSE2	

*: For details of the package, see "Package Dimensions".

15. Package Dimensions

Package Type	Package Code
LQFP 144pin	LQS144



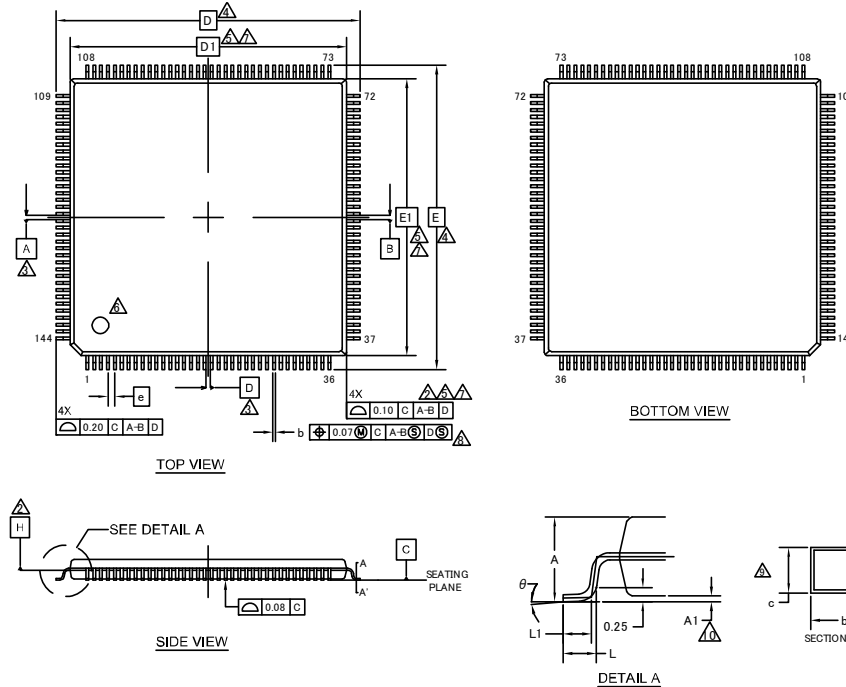
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

- NOTES**
- ALL DIMENSIONS ARE IN MILLIMETERS
 - DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
 - DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
 - DATUMS A-B AND D TO BE DETERMINED AT SEATING PLANE C.
 - DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
 - DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
 - REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
 - DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
 - THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
 - A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 *A

PACKAGE OUTLINE. 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 REV#A

Package Type	Package Code
LQFP 144pin	LQN144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.145	0.18	0.215
c	0.115	—	0.195
D	18.00 BSC		
D1	16.00 BSC		
e	0.40 BSC		
E	18.00 BSC		
E1	16.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

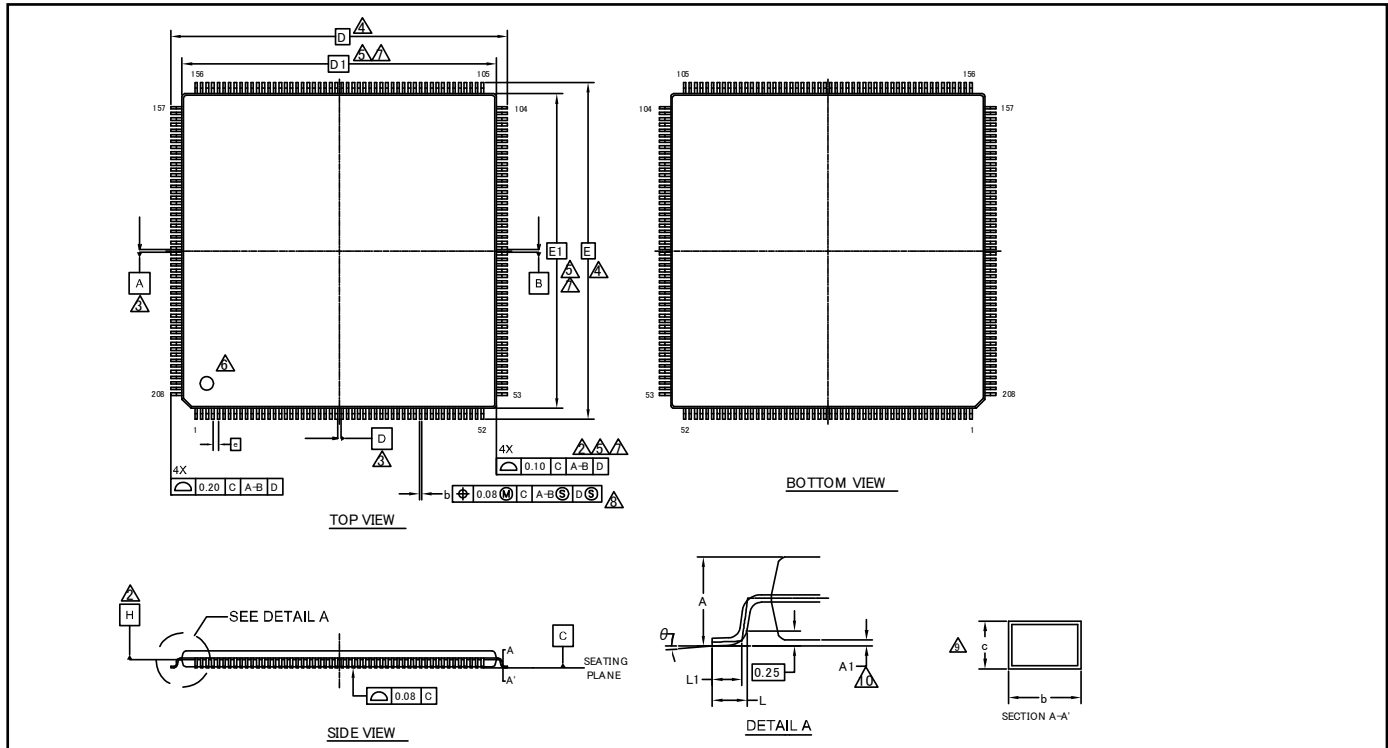
NOTES

- CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-14045 **

 PACKAGE OUTLINE, 144 LEAD LQFP
 16.0X16.0X1.7 MM LQN144 REV**

Package Type	Package Code
LQFP 208pin	LQR208



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	30.00 BSC		
D1	28.00 BSC		
e	0.50 BSC		
E	30.00 BSC		
E1	28.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (⊗) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15151 **

PACKAGE OUTLINE, 208 LEAD LQFP
28.0X28.0X1.7 MM LQR208 REV**

16. Major Changes

Spanion Publication Number: DS705-00009

Page	Section	Change Results
Revision 2.0		
-	-	Initial release
Revision 2.1		
-	-	Company name and layout design change
Revision 2.2		
-	P104-P108	Revised text position

Note: Please see “Document History” about later revised information.

Document History

Document Title: CY91570 Series 32-bit Microcontroller

Document Number: 002-04725

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NNAS	06/19/2015	Migrated to Cypress and assigned document number 002-04725. No change to document contents or format.
*A	5174263	NNAS	03/16/2016	Updated to Cypress format.
*B	6542252	TORS	04/24/2019	Changed series name and part number: MB91570 -> CY91570 Changed package dimensions. Updated Ordering Information.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Videos](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

© Cypress Semiconductor Corporation 2013-2019. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Infineon:](#)

[CY91F575BHSPMC-GSE1](#) [CY91F579CHSPMC1-GSE1](#) [CY91F577BPMC-GSE2](#) [CY91F577BHSPMC1-GSE1](#)
[CY91F579CMPMC-GSE2](#) [CY91F575BPMC-GSE2](#) [CY91F577BHSPMC-GSE1](#) [CY91F579CHSPMC-GSE1](#)