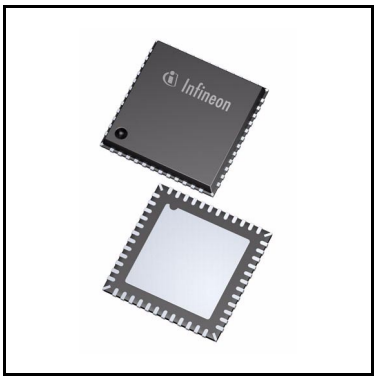
TLE92104-232

Multiple MOSFET Driver IC

AEC Qualified

RoHS



1 Overview

Features

- Four half-bridge gate drivers for external N-channel MOSFETs
- Control of reverse battery protection MOSFET
- Adaptive MOSFET gate control
  - Improved electromagnetic emission
  - Reduced switching losses in PWM mode
- 24-bit Serial Peripheral Interface
- Two current sense amplifiers with configurable gain
  - High-side and low-side capable for protection and diagnosis
- Drain-source monitoring for short circuit detection
- Overtemperature warning and shutdown
- Timeout watchdog
- Detailed off-state diagnostic (open load, short circuit to battery or short circuit to GND) via SPI
- Three PWM inputs
  - High-side and low-side PWM capable
  - Active free-wheeling
  - Up to 25 kHz PWM frequency
- Low current consumption in sleep mode
- Configurable low-side 1-4 brake with short circuit detection in sleep mode and normal mode
- Configurable VS overvoltage detection in sleep mode
- Leadless power package with support of optical lead tip inspection
- Green Product (RoHS compliant)
- AEC Qualified

Potential applications

- Seat control and extended functions (steering column adjustment, gas pedal adjustment)
- Power lift gate
- Central door lock
- Body control module (cargo cover, washer pump, window lift, rear wiper ...)

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE92104-232 is a Multi-MOSFET driver IC dedicated to control up to eight n-channel MOSFETs. It includes four half-bridges for DC motor control applications such as automotive power seat control or other applications.

A 24-bit Serial Peripheral Interface (SPI) is used to configure the TLE92104-232 and to control the half-bridges. It also allows the read out of the status registers for diagnostic purpose.

The TLE92104-232 offers a wide range of diagnostic features such as the monitoring of the supply voltage, the charge pump voltage, temperature warning and over-temperature shutdown. Each gate driver monitors independently its external MOSFET drain-source voltage for fault conditions.

The device is housed in a VQFN-48 with exposed pad supporting lead tip inspection. The package provides a good thermal performance and minimizes the required PCB space.

Type	Package	Marking
TLE92104-232	PG-VQFN-48	TLE92104-232QX

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2 Block diagram

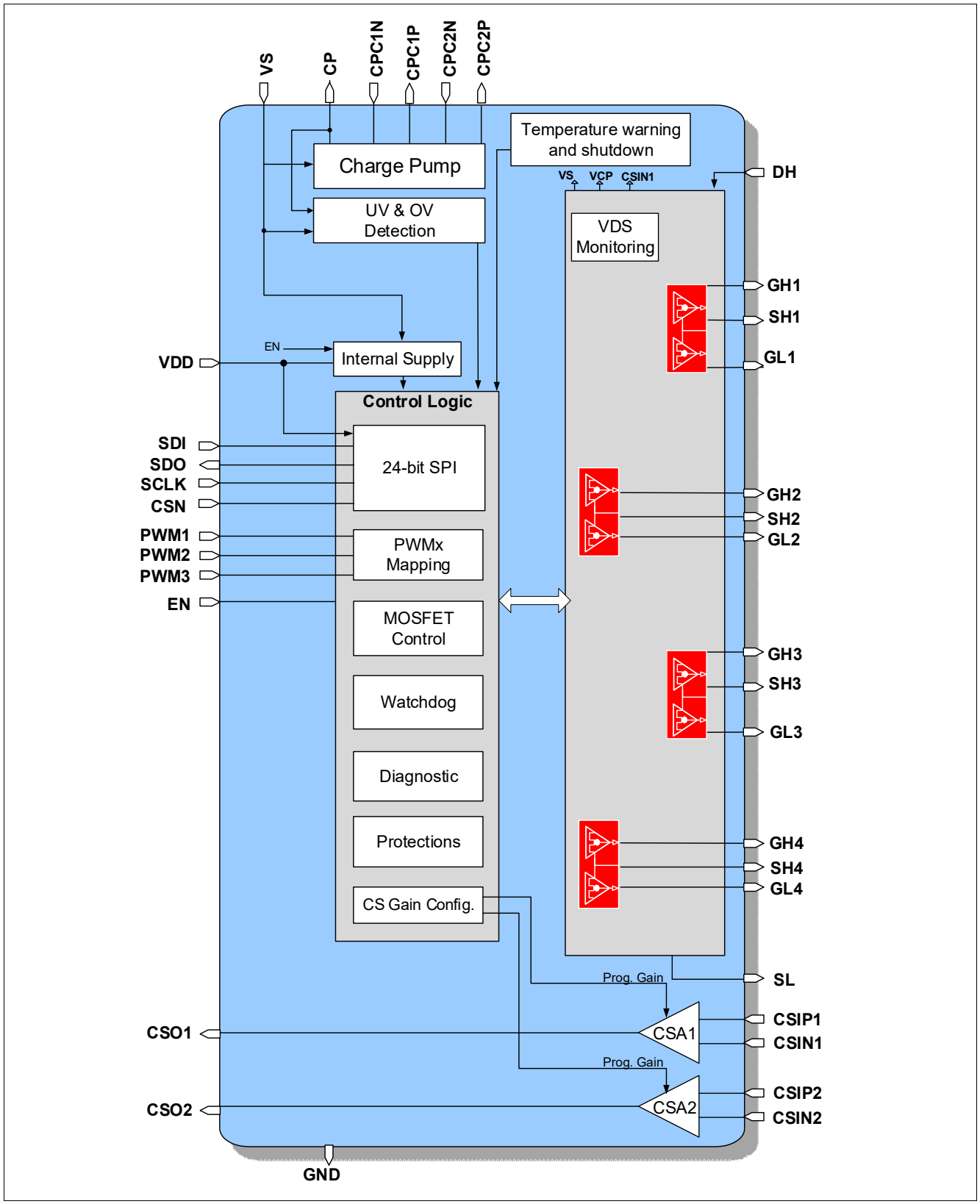


Figure 1 Block diagram

2.1 Voltage and current definition

Figure 2 shows terms used in this datasheet, with associated convention for positive value.

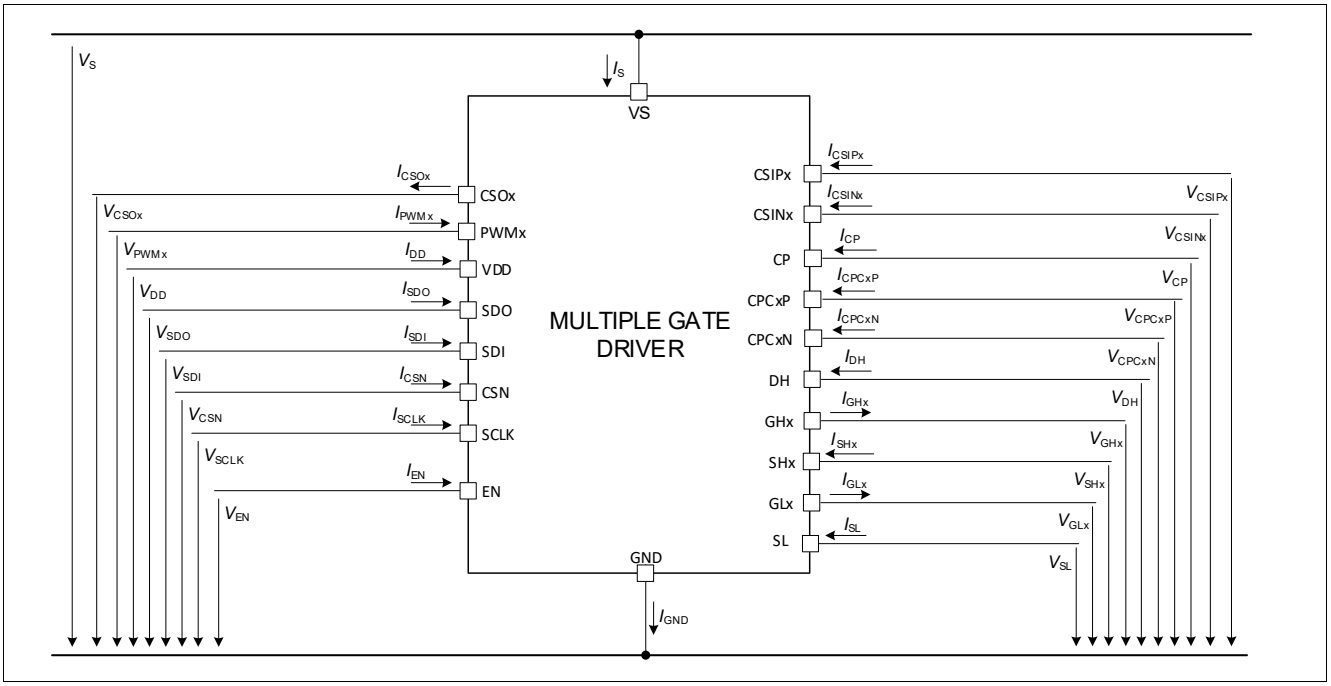


Figure 2 Voltage and current definition

3 Pin configuration

3.1 Pin assignment

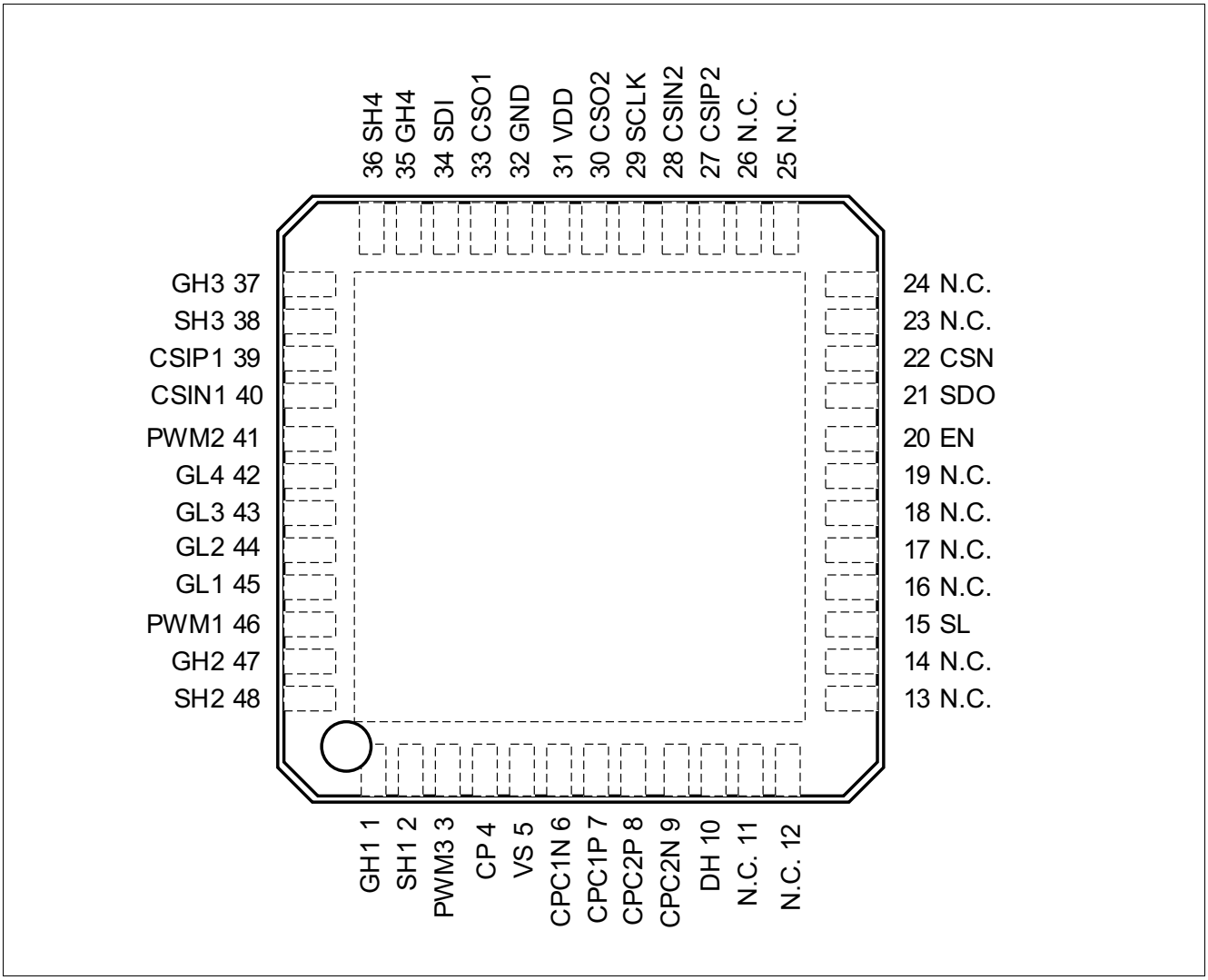


Figure 3 Pin configuration TLE92104-232QX

3.2 Pin definitions and functions

Table 1 Pin configuration TLE92104-232QX

Pin	Symbol	Function
1	GH1	**Gate high-side 1** Analog I/O pin to turn on/off high-side MOSFET 1. Connect to the gate of high-side MOSFET 1.
2	SH1	**Source high-side 1** Connection to source of high-side MOSFET 1.
3	PWM3	**PWM input 3**
4	CP	**Charge Pump Output**
5	VS	**Supply Voltage** Device supply voltage. Connect this pin to the supply (battery) voltage with a reverse battery protection circuit.
6	CPC1N	**Negative connection to Charge Pump Capacitor 1**
7	CPC1P	**Positive connection to Charge Pump Capacitor 1**
8	CPC2P	**Positive connection to Charge Pump Capacitor 2**
9	CPC2N	**Negative connection to Charge Pump Capacitor 2**
10	DH	**Drain input for high-sides** Input for the drains of high-side MOSFETs. Refer to **Chapter 7.3**.
11	N.C.	Not connected
12	N.C.	Not connected
13	N.C.	Not connected
14	N.C.	Not connected
15	SL	**Source low-side** Common connection to the source of the low-side MOSFETs.
16	N.C.	Not connected
17	N.C.	Not connected
18	N.C.	Not connected
19	N.C.	Not connected
20	EN	**Enable input** with internal pull-down
21	SDO	**Serial Data Output**
22	CSN	**Chip Select Not** with internal pull-up
23	N.C.	Not connected
24	N.C.	Not connected
25	N.C.	Not connected
26	N.C.	Not connected
27	CSIP2	**Non-Inverting input of the Current Sense Amplifier 2**
28	CSIN2	**Inverting input of the Current Sense Amplifier 2**
29	SCLK	**Serial Clock Input** with internal pull-down
30	CSO2	**Current Sense Amplifier Output 2**

Pin configuration

Table 1 Pin configuration TLE92104-232QX

Pin	Symbol	Function
31	VDD	**Logic supply**
32	GND	**Ground connection**
33	CSO1	**Current Sense Amplifier Output1**
34	SDI	**Serial Data Input with internal pull-down**
35	GH4	**Gate high-side 4**
36	SH4	**Source high-side 4**
37	GH3	**Gate high-side 3**
38	SH3	**Source high-side 3**
39	CSIP1	**Non-inverting input of the Current Sense Amplifier 1**
40	CSIN1	**Inverting input of the Current Sense Amplifier 1** . This pin can be used as reference for the high-side MOSFET drain if CSA1 is configured as high-side. Refer to **Chapter 7.3**
41	PWM2	**PWM input 2**
42	GL4	**Gate low-side 4**
43	GL3	**Gate low-side 3**
44	GL2	**Gate low-side 2**
45	GL1	**Gate low-side 1**
46	PWM1	**PWM input 1**
47	GH2	**Gate high-side 2**
48	SH2	**Source high-side 2**
	E.P.	**Exposed pad** For cooling purpose only, do not use as electrical GND[1)].

1) The exposed pad at the bottom of the package allows better power dissipation from TLE92104-232 via the PCB. The exposed pad must be left floating or connected to GND (recommended) for best EMC and thermal performance.

4 General product characteristics

4.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1)]

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V	–	P_4.1.1
PWM input voltages (PWMx)	V_{PWMx}	-0.3	–	V_{DD} + 0.3	V	$\|I\|$< 10 mA	P_4.1.2
Logic input voltages (SDI, SCLK, CSN, EN)	V_{SDI}, V_{SCLK}, V_{CSN}, V_{EN}	-0.3	–	V_{DD} + 0.3	V	$\|I\|$< 10 mA	P_4.1.3
Voltage range and SDO	V_{SDO}	-0.3	–	V_{DD} + 0.3	V	$\|I\|$< 10 mA	P_4.1.4
Voltage range at CSIPx and CSINx	V_{CSIP}, V_{CSIN}	-8.0	–	40	V	–	P_4.1.5
Differential input voltage range CSIPx - CSINx	$V_{CSIDiff}$	-8.0	–	8.0	V	–	P_4.1.21
Voltage range at DH	V_{DH}	-0.3	–	40	V	–	P_4.1.6
Voltage range at SL	V_{SL}	-8.0	–	6.0	V	–	P_4.1.7
Voltage range at SHx	V_{SH}	-8.0	–	40	V	–	P_4.1.8
Voltage range at GHx	V_{GH}	-8.0	–	40	V	–	P_4.1.9
Voltage range at GLx	V_{GL}	-8.0	–	24	V	–	P_4.1.10
Voltage difference between GLx and SL	V_{GS_LS}	-0.3	–	16	V	–	P_4.1.11
Voltage difference between GHx and SHx	V_{GS_HS}	-1.0	–	16	V	2)	P_4.1.23
Voltage range at charge pump pins CP	V_{CP}	V_S-0.3	–	V_S+17	V	–	P_4.1.12
Voltage range at charge pump pins CPC1P, CPC2P	V_{CPCxP}	-0.3	–	V_S+17	V	–	P_4.1.22
Voltage range at charge pump pins CPC1N, CPC2N	V_{CPCxN}	-0.3	–	V_S+0.3	V	–	P_4.1.24
Logic supply voltage	V_{DD}	-0.3	–	5.5	V	–	P_4.1.13
Voltage at CSOx	V_{CSOx}	-0.3	–	V_{DD} + 0.3	V	–	P_4.1.14
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	

Table 2 Absolute maximum ratings[1)] (cont'd)

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.16
ESD susceptibility							
ESD susceptibility all pins	$V_{ESDHBM1}$	-2	–	2	kV	HBM[3)]	P_4.1.17
ESD susceptibility of VS and DH pins versus GND	$V_{ESDHBM2}$	-4	–	4	kV	HBM[3)]	P_4.1.18
ESD susceptibility all pins	$V_{ESDCDM1}$	-500	–	500	V	CDM[4)]	P_4.1.19
ESD susceptibility pin corner pins	$V_{ESDCDM2}$	-750	–	750	V	CDM[4)]	P_4.1.20

1) Not subject to production test, specified by design.
2) V_{GS_GH} may be between -1.0 and -0.3V only if the current injected into SHx is below 4 mA
3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
4) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(nor)}$	6.0	–	28	V	–	P_4.2.1
Extended supply voltage range	$V_{S(ext)}$	5.5	–	6	V	[1)] Parameter deviations possible	P_4.2.7
Extended supply voltage range	$V_{S(ext)}$	28	–	V_{SOV_OFF2} (max)	V	[1)] Parameter deviations possible	P_4.2.2
Supply voltage transients slew rate	dV_S/dt	-10	–	10	V/µs	[1)]	P_4.2.3
Logic supply voltage	V_{DD}	3.0	–	5.5	V	–	P_4.2.4

Table 3 Functional range (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SPI logic input voltage	V_{SDI}, V_{SCLK}, V_{CSN}	0	–	V_{DD}	V	–	P_4.2.5
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.6

1) Not subject to production test, specified by design.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	7.1	–	K/W	1)	
Junction to ambient	R_{thJA}	–	31	–	K/W	1)2)	

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

5 General description

5.1 Power supply

The Multiple MOSFET Driver IC requires two power supplies: V_S and V_{DD}.

V_{DD} supplies the I/O buffers (including the SPI pins) and the internal voltage regulator for the logic. V_{DD} allows the flexibility of a 3.3 V or a 5.0 V logic interface.

V_S supplies the charge pump for the MOSFET gate drivers. The V_S pin must be connected to the battery through a reverse battery protection.

Both supplies are separated so that the information stored in the logic remains intact in the event of voltage drop on V_S. V_{DD} and V_S should be decoupled with ceramic capacitors connected close to the supply and ground planes.

5.2 Operation modes

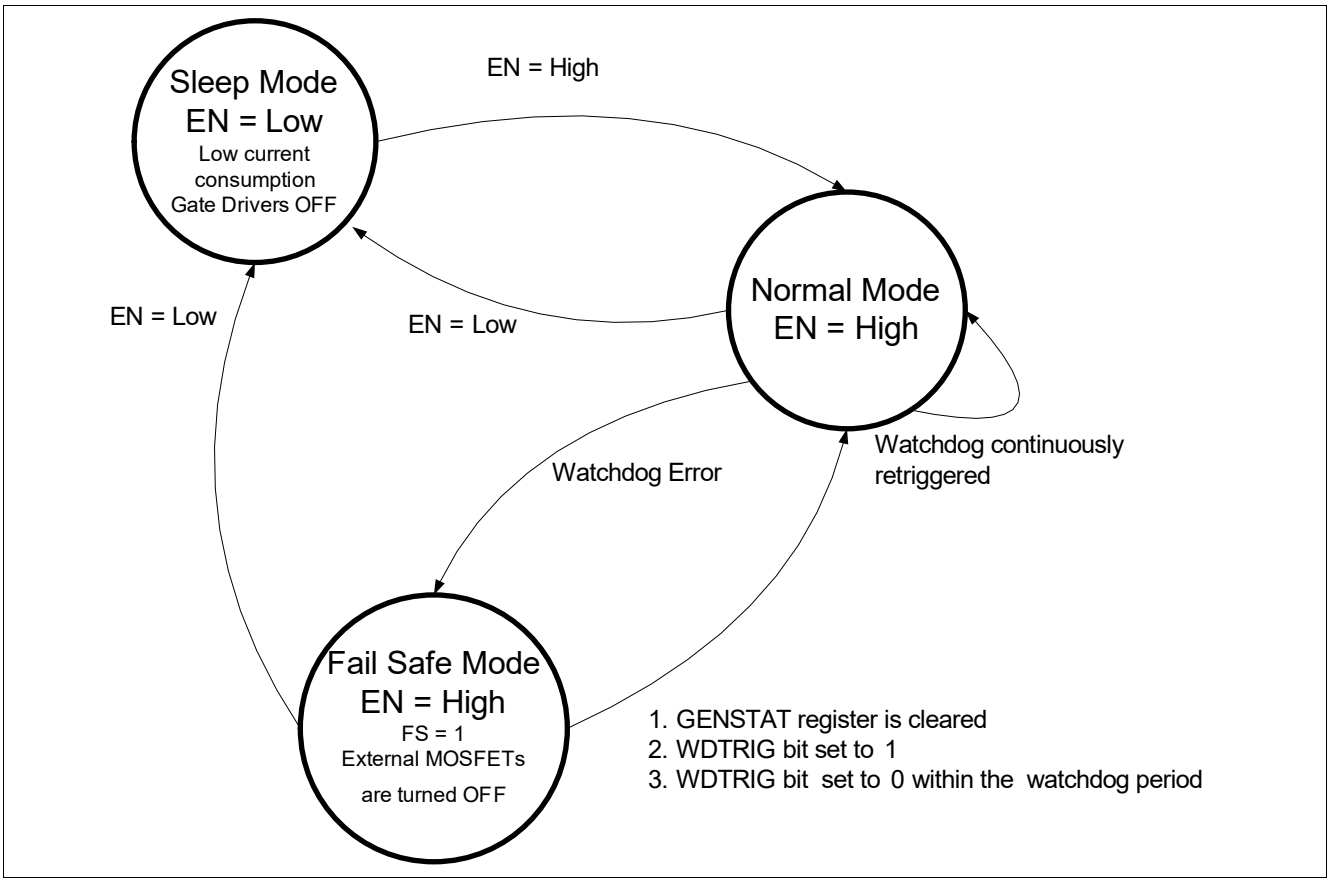


Figure 4 State diagram

*Note: The state diagram is valid for V_S and V_{DD} within the nominal operating range. For V_S and V_{DD} outside of the nominal range, refer to **Chapter 7.8**, respectively **Chapter 5.2.2**.*

5.2.1 Normal mode

The TLE92104-232 enters Normal Mode by setting EN pin to High and waiting for the SPI setup time t_{SET_SPI}. In normal mode, the MOSFET gate drivers are enabled and can be configured through the SPI interface, provided

that the voltages applied to V_{DD} and V_S are within the operating range. The watchdog must be retriggered correctly in order to stay in Normal Mode (see **Chapter 7.10**).

5.2.2 Sleep mode

The Multiple MOSFET Driver IC enters Sleep Mode by setting EN pin to Low. The transition to the sleep mode is delayed by t_{DSLEEP}[1] (max tCCP of active half-bridges + 3 µs) in order to actively turn-off the external MOSFETs. In this mode, the internal regulator and the internal circuitry are deactivated, and the SPI registers are reset.
The current consumption of V_{DD} is reduced to I_{DD_Q}. The current consumption of V_S is reduced to I_{SQ} or I_{SQ} + I_{SQ_BRAKE}.

The V_S current consumption is I_{SQ} if:

- **PASS_MOD** = 00_B and **PASS_VDS** = 0_B while entering sleep mode
- and V_S never drops below V_{SLEEP_SET} after entering sleep mode

The V_S current consumption is I_{SQ} + I_{SQ_BRAKE} if:

- **PASS_MOD** = 01_B, 10_B, 11_B or **PASS_VDS** = 1_B while entering sleep mode
- or V_S has recovered from a voltage below V_{SLEEP_SET} (i.e. V_S has ramped up from a voltage below V_{SLEEP_SET} or V_S has dropped below V_{SLEEP_SET})

The internal resistors R_{GGND} between GHx/GLx and GND are activated to discharge the gate of the external MOSFETs.

Note: If EN is set to Low for a duration shorter than (t_{ENL_FILT}, 8 µs max.), and EN is set to High again, then device does not go in sleep mode and the registers are not reset. The half-bridges are reactivated according to the settings of the control registers when EN is High.

5.2.3 Fail Safe Mode

In case of watchdog error (see **Chapter 7.10**), the device enters Fail Safe Mode, FS bit is set (see **Global status byte**) and the external MOSFETs are actively discharged with the static discharge current (**Chapter 6.2**) during the max. configured tHBxCCP active (**Chapter 7.5.1**). Then the bridge driver is set to passive mode (the passive discharge path is activated,**Chapter 6.4**, all external MOSFETs are latched off, and the charge pump is deactivated). To resume Normal Mode the microcontroller must execute the following sequence[2]:

1. Clear **GENSTAT** register.
2. Write WDTRIG bit to 1 (**GENCTRL1**) within the watchdog period.
3. Write WDTRIG bit to 0 within the watchdog period[3].

In fail safe mode, the control registers are frozen to their default value, at the exception of **WDTRIG**, **CCSO**, **PASS_VDS**, **PASS_MOD**, **CSA1L**, **CSA2L**. Any write command (except for WDTRIG bit) or clear command (except for GENSTAT) will be discarded in this mode and sets SPIE bit (**Global status byte**).

A clear command to **GENSTAT** in fail safe mode does not reset any failure flag reported by this status register.

1) SPI Frames are ignored during t_{DSLEEP}.
2) The exit sequence must be strictly followed to leave fail safe mode. If a SPI frame not belonging to the sequence is added, then the device stays in fail safe mode and the microcontroller must restart the complete sequence to enter normal mode.
3) During Fail Safe Mode, the charge pump is deactivated and **CPUV** is set. Therefore, recovering from Fail Safe Mode, **GENSTAT** must be cleared again at the end of the Fail Safe exit sequence to re-activate of the gate drivers.

The control and status registers can be read in this mode before the start of the exit sequence without SPIE bit being set.

5.3 Reset behavior

The following events trigger a Power On Reset:

V_{DD} undervoltage reset:

If $V_{DD} < V_{DD\ PoffR}$ the digital block is deactivated and the outputs are switched off. The digital block is reset once $V_{DD} > V_{DD\ POR}$. Then NPOR bit (negated power-on reset bit, see **Global status byte**) is reset to 0 to report the reset condition.

Reset on EN pin:

If the EN pin is pulled low, the logic content is reset and the device enters sleep mode. Once the device enters Normal Mode (after t_{SET_SPI} with EN = high and $V_{DD} > V_{DD\ POR}$), the NPOR bit is reset to 0 to report the reset condition.

NPOR is set to 1 when **GENSTAT** is cleared.

5.4 Charge pump

A dual-stage charge pump supplies the gate drivers for the high-side and low-side MOSFETs. It requires three external capacitors connected between CPC1N and CPC1P, CPC2N and CPC2P, VS and CP.

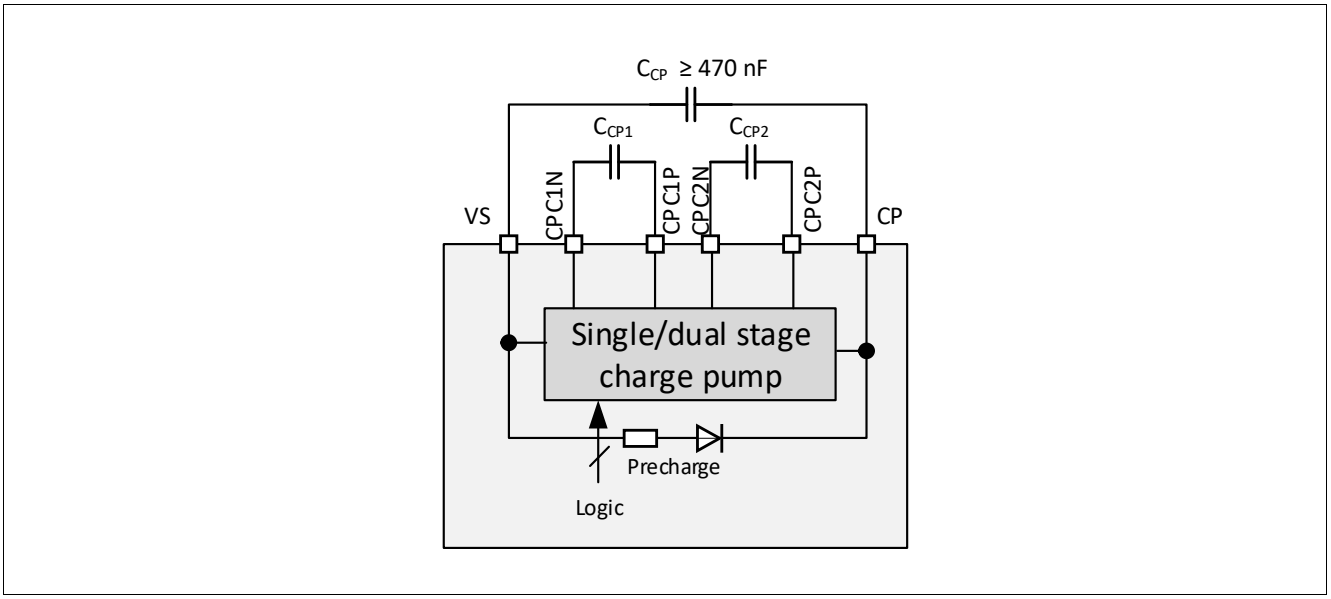


Figure 5 Charge pump

CPSTGA = 0 (default, see **GENCTRL2**), the device operates with the dual-stage charge pump.

If CPSTGA = 1 (**GENCTRL2**), the device switches automatically to single-stage or dual-stage charge pump automatically:

- If $V_S > V_{CPSO\ DS}$: the TLE92104-232 switches from a dual-stage to a single-stage charge pump.
- If $V_S < V_{CPSO\ SD}$: the TLE92104-232 switches from single-stage to dual-stage charge pump.

The operation with the single-stage charge pump reduces the current consumption from the VS pin.

5.5 Frequency modulation

A modulation of the charge pump frequency can be activated to reduce the peak emission. The modulation frequency can be selected based on the resolution bandwidth of the peak detector during EMC testing.

The modulation frequency is set by the control bit FMODE in **GENCTRL1**

- FMODE = 0: No modulation.
- FMODE = 1: Modulation frequency = 15.6 kHz (default).

5.6 Electrical characteristics

5.6.1 Electrical characteristics: supply

Table 5 Electrical characteristics: supply

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption, EN = LOW)							
Supply quiescent current	I_{SQ}	–	2	5	µA	T_j < 85°C, V_S= 13.5 V **PASS_MOD**=00_B, **PASS_VDS**=0_B	P_5.5.1
Supply quiescent current	I_{SQ2}	–	5	7	µA	T_j < 85°C, V_S< 25 V **PASS_MOD**=00_B,**PASS_VDS**=0_B	P_5.5.61
Additional supply quiescent current, brake enabled	I_{SQ_BRAKE}	–	5	7.5	µA	T_j < 85°C, V_S = 13.5 V [1] **PASS_MOD**=01_B or 10_Bor 11_B or **PASS_VDS**=1_B	P_5.5.60
Logic Supply quiescent current	I_{DD_Q}	–	1	3	µA	T_j < 85°C	P_5.5.3
Total quiescent current	I_{DD_Q} + I_{SQ}	–	3	8	µA	T_j < 85°C, V_S= 13.5 V **PASS_MOD**=00_B, **PASS_VDS**	P_5.5.5
EN Low filter time	t_{DSLEEP}	–	–	Max. tCCP + 3 µs	µs	[2)3)] **BD_PASS** = 0	P_5.5.49
EN Low filter time	t_{ENL_FILT}	1	–	8	µs	[2)]	P_5.5.51
VS for LS1-4 setting	V_{SLEEP_SET}	–	–	5.5	V		P_5.5.63
Current consumption, EN = HIGH							
Supply current	I_{S1}	–	45	55	mA	HBxVDSTH = 001_B, **BD_PASS** = 0, I_{CP} = 0 mA	P_5.5.6
Supply current	I_{S2}	–	83	100	mA	8 V < V_S < 28 V HBxVDSTH = 001_B, **BD_PASS** = 0, I_{CP} = -12 mA, dual stage CP	P_5.5.7

Table 5 Electrical characteristics: supply (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply current	I_{S3}	–	55	70	mA	18 V < V_S < 28 V HBxVDSTH = 001_B, **BD_PASS** = 0, I_{CP} = -12 mA[2], single stage CP	P_5.5.56
Supply current	I_{S4}	–	55	70	mA	V_S = 6 V, HBxVDSTH = 001_B, **BD_PASS** = 0, I_{CP} = - 6 mA[2]	P_5.5.57
Supply current	$I_{S\_BD\_PASS}$	–	10	20	mA	HBxMODE=00_B, **BD_PASS** = 1	P_5.5.54
Logic supply current	I_{DD1}	–	3	4	mA	SPI not active, CSA1 and CSA2 off, all I_{PDDiag} off, **BD_PASS**=0	P_5.5.8
Logic supply current	I_{DD2}	–	3	3.8	mA	[4] Additional VDD current per CSA on, VCSOx = 4.5 V, LS shunt, **CCSO** = 1 CSAxL = 0, I_{PDDiag} off	P_5.5.52
Logic supply current	I_{DD3}	–	2	2.8	mA	[4] Additional VDD current per CSA on, **CCSO** = 0, VCSOx = 4.5 V, LS shunt, CSAxL = 0, I_{PDDiag} off	P_5.5.55
Logic supply current	I_{DD4}	–	6	7	mA	[5] Additional VDD current per CSA on, VCSOx = 4.5 V, HS shunt, **VSOVTH** = 1 CSAxL = 1, I_{PDDiag} off	P_5.5.58
Logic supply current	I_{DD5}	–	4.2	5.2	mA	[5] Additional VDD current per CSA on, **VSOVTH** = 0, VCSOx = 4.5 V, HS shunt, CSAxL = 1, I_{PDDiag} off	P_5.5.59

Table 5 Electrical characteristics: supply (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Additional logic supply current pull-down	I_{DD_PDDiag}	–	1.5	2	mA	Additional VDD current when all I_{PDDiag} are on	P_5.5.53
VS with active bridge driver (BD_PASS = 0)							
UV switch ON voltage	$V_{SUV\ ON}$	–	–	5.5	V	V_S increasing	P_5.5.11
UV switch OFF voltage	$V_{SUV\ OFF}$	4.0	4.5	5.0	V	V_S decreasing	P_5.5.12
UV ON/OFF hysteresis	$V_{SUV\ HY}$	–	0.5	–	V	$V_{SUV\ ON}$ - $V_{SUV\ OFF}$ 2)	P_5.5.13
OV switch OFF voltage VSOVTH = 0	$V_{SOV\ OFF1}$	19	–	21	V	V_S increasing	P_5.5.14
OV switch ON voltage VSOVTH = 0	$V_{SOV\ ON1}$	18	–	20	V	V_S decreasing	P_5.5.15
OV switch OFF voltage VSOVTH = 1	$V_{SOV\ OFF2}$	29	–	31	V	V_S increasing	P_5.5.16
OV switch ON voltage VSOVTH = 1	$V_{SOV\ ON2}$	28	–	30	V	V_S decreasing	P_5.5.17
OV ON/OFF hysteresis	$V_{SOV\ HY}$	–	1	–	V	$V_{SUV\ ON}$ - $V_{SUV\ OFF}$ 2)	P_5.5.18
VS undervoltage filter time	t_{VSUV_FILT}	7	10	13	µs	1)	P_5.5.47
VS overvoltage filter time	t_{VSOV_FILT}	7	10	13	µs	2)	P_5.5.48
CP turn-off delay after VS overvoltage detection	t_{D_CPVSOV}	12.8	16	19.2	µs	2)	P_5.5.50
VDD							
V_{DD} Power-On-Reset	$V_{DD\ POR}$	2.40	2.60	2.80	V	V_{DD} increasing	P_5.5.19
V_{DD} Power-Off-Reset	$V_{DD\ POffR}$	2.30	2.50	2.70	V	V_{DD} decreasing	P_5.5.20
V_{DD} Power-On-Reset Hysteresis	$V_{DD\ POR\ HY}$	–	0.1	–	V	$V_{DD\ POR}$ - $V_{DD\ POffR}$ 2)	P_5.5.21

1) Additional quiescent current if VS drops below V_{SLEEP_SET}.
2) Not subject to production test, specified by design.
3) Max. cross-current protection time of the active half-bridges.
4) Parameter independent of **VSOVTH**.
5) Parameter independent of **CCSO**.

5.6.2 Electrical characteristics: logic inputs PWMx, EN

Table 6 Electrical characteristics: PWMx, EN

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
EN high voltage	V_{ENH}	0.7 × V_{DD}	–	–	V	–	P_5.5.22
EN low voltage	V_{ENL}	–	–	0.3 × V_{DD}	V	–	P_5.5.23
EN hysteresis	V_{ENHY}	–	0.12 × V_{DD}	–	V	1)	P_5.5.24
EN pull-down resistor	R_{PD_EN}	30	40	50	kΩ	–	P_5.5.25
PWMx high voltage	V_{PWMH}	0.7 × V_{DD}	–	–	V	–	P_5.5.26
PWMx low voltage	V_{PWML}	–	–	0.3 × V_{DD}	V	–	P_5.5.27
PWMx hysteresis	V_{PWMHY}	–	0.12 × V_{DD}	–	V	1)	P_5.5.28
PWMx pull-down resistor	R_{PD_PWMx}	30	40	50	kΩ	–	P_5.5.29

1) Not subject to production test, specified by design.

5.6.3 Electrical characteristics charge pump

Table 7 Electrical characteristics: charge pump

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Charge Pump Frequency	f_{CP}	–	250	–	kHz	3)	P_5.5.30
Output Voltage VCP vs. VS	V_{CPmin}	8.5	–	–	V	V_S = 6 V, I_{CP} = - 6 mA	P_5.5.31
Regulated output voltage VCP vs. VS, CPSTGA = 0	V_{CP1}	11	15	17	V	8 V < V_S < 28 V, I_{CP} = - 12 mA	P_5.5.32
Regulated output voltage VCP vs. VS, CPSTGA = 1	V_{CP2}	12	15	17	V	18 V < V_S < 28 V, I_{CP} = - 12 mA	P_5.5.41
Turn-on time, CPSTGA = 0	t_{ON_VCP1}	10	40	80	µs	8 V < V_S < 28 V (25%)[1)2)3)4)]	P_5.5.34
Rise time, CPSTGA = 0	t_{RISE_VCP1}	10	60	100	µs	8 V < V_S < 28 V (25%-75%)[1)2)3)4)]	P_5.5.35
Turn-on time, CPSTGA = 1	t_{ON_VCP2}	10	40	80	µs	18 V < V_S < 28 V (25%)[1)2)3)5)]	P_5.5.36

Table 7 Electrical characteristics: charge pump

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Rise time, CPSTGA = 1	t_{RISE_VCP2}	10	60	100	µs	18 V < V_S < 28 V (25%-75%)[1)2)3)5)]	P_5.5.37
Charge Pump Undervoltage (referred to VS)	V_{CPUV1}	5.5	6	6.5	V	**CPUVTH** = 0, VCP falling	P_5.5.38
Charge Pump Undervoltage (referred to VS)	V_{CPUV2}	7	7.5	8	V	**CPUVTH** = 1, VCP falling	P_5.5.42
Automatic switch over dual to single stage charge pump	$V_{CPSO\ DS}$	16	17	18	V	**CPSTGA** = 1	P_5.5.43
Automatic switch over single to dual stage charge pump	$V_{CPSO\ SD}$	15.5	16.5	17.5	V	**CPSTGA** = 1	P_5.5.44
Charge pump switch over hysteresis	$V_{CPSO\ HY}$	–	0.5	–	V	3) **CPSTGA** = 1, $V_{CPSO\ DS}$ - $V_{CPSO\ SD}$	P_5.5.45
Charge Pump Undervoltage Filter Time	t_{CPUV}	51	64	77	µs	3)	P_5.5.39
Charge pump minimum output current	I_{CPOC1}	–	–	-12	mA	2)3)4) V_S = 13.5 V; **CPSTGA** = 0	
Charge pump minimum output current	I_{CPOC2}	–	–	-12	mA	2)3)5) V_S = 18 V; **CPSTGA** = 1	

1) Parameter dependent on the capacitance C_{CP}.
2) C_{CPC1} = C_{CPC2} = 220 nF, C_{CP} = 470 nF, I_{CP} = 0 mA.
3) Not subject to production test, specified by design.
4) Dual stage charge pump.
5) Single stage charge pump.

6 Floating gate drivers

The TLE92104-232 integrates eight floating gate drivers capable of controlling a wide range of n-channel MOSFETs. They are configured as four high-sides and low-sides, building four half-bridges.

This section describes the MOSFET control by the gate drivers.

After power-on reset, the bridge driver is in passive mode (default value of **BD_PASS** = 1 and all HBxMODE=00_B). Refer to **Chapter 6.4** and **Chapter 6.5**.

The bridge driver is in active mode by setting **BD_PASS** to 0. **Chapter 6.1**, **Chapter 6.2** and **Chapter 6.3** describes the static and PWM control in active mode.

Attention: It is highly recommended to have all HBxMODE bits set to 00_B or 11_B before setting BD_PASS to 0 in order to avoid wrong drain-source overvoltage detection.

Table 8 Operating modes of the gate driver

EN	BD_PASS	HBxMODE[1:0]	Gate driver	Comment	Chapter
High	0	x	Active[1)]		**Chapter 6.1** **Chapter 6.2** **Chapter 6.3**
High	1	One HBxMODE = 01_B or 10_B	Active[1)]	Equivalent to EN=High and **BD_PASS** = 0	**Chapter 6.1** **Chapter 6.2** **Chapter 6.3**
High	1	All HBxMODE=00_B or 11_B	Passive		**Chapter 6.5**
Low	x	x	Passive		**Chapter 6.5**

1) Provided that no VS overvoltage, VS undervoltage, CP undervoltage or overtemperature failure are detected, and TLE92104-232 is not in Fail Safe Mode.

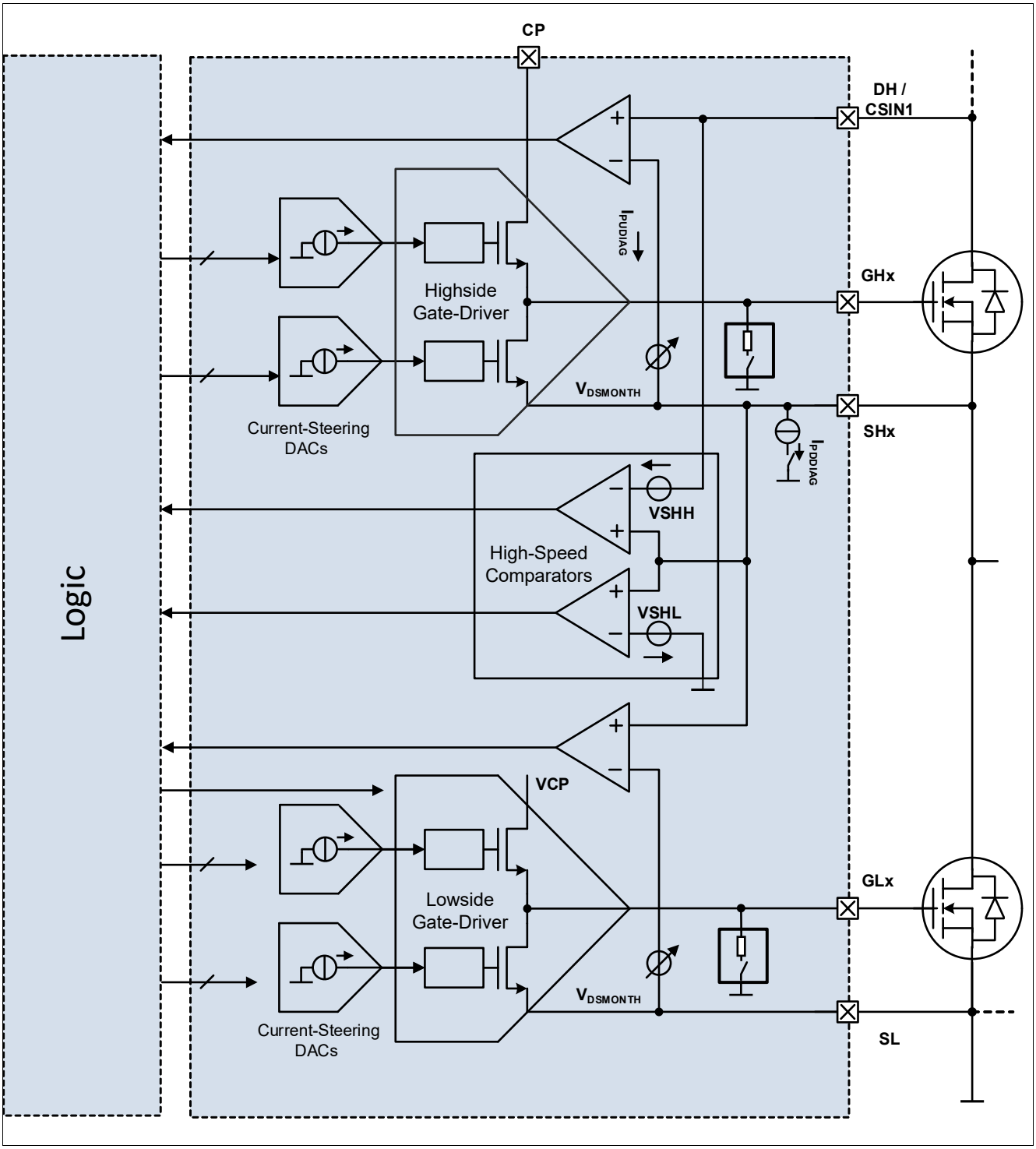


Figure 6 Block diagram - Gate driver for one half-bridge

6.1 MOSFET control with bridge driver in active mode (BD_PASS = 0 and EN = High)

Depending on the configuration bits HBxMODE[1:0] (**HBMODE**, **Table 9** and **Table 11**), each high-side and low-side MOSFETs can be:

- deactivated
- activated (statically, no PWM)
- activated in PWM mode (**Chapter 6.3**, **PWMSET**)

Table 9 Half-bridge mode selection

HBxMODE[1:0][1)]	Configuration of HSx/LSx[1)]
00_B	LSx and HSx MOSFETs are actively kept OFF (default)
01_B	LSx MOSFET is ON (static or PWM, refer to **Table 11**), HSx MOSFET is actively kept OFF
10_B	HSx MOSFET is ON (static or PWM, refer to **Table 11**), LSx MOSFET is actively kept OFF
11_B	Reserved - LSx and HSx MOSFETs are actively kept OFF

1) x = 1 … 4.

6.2 Static activation with bridge driver in active mode (BD_PASS = 0)

In this section, we consider the static activation of the high-side and low-side MOSFET of the half-bridge x, x = 1…4. Refer to **Table 11** for the setting of a high-side or low-side in the static or PWM operation.

If HBx is not mapped to any activated PWM channel, the low-side or high-side MOSFET of HBx is statically activated (no PWM) by setting HBxMODE[1:0] to respectively (0,1) or (1,0).

The configured cross-current protection and the Drain-Source overvoltage blank times for the Half-Bridge x are noted $t_{HBxCCP\ Active}$ and $t_{HBxBLANK\ Active}$ (refer to **Chapter 7.5**).

The charge and discharge currents applied to the static controlled Half-Bridge x are noted ICHGSTx (**ST_ICHG**).

IHARDOFF is the maximum current that the gate drivers can sink. It corresponds to the discharge current when IDCHGx[4:0] = 31_D (See **PWM_IDCHG_ACT**). This current is used to the keep a MOSFET off, when the opposite MOSFET of the same half-bridge is being turned on. This feature avoids parasitic cross-current conduction.

ICHGSTx is the current sourced, respectively sunk, by the gate driver to turn-on the high-side x or low-side x. ICHGSTx is configured in the control register **ST_ICHG**.

Table 10 Static charge and discharge currents

ICHGSTx[3:0][1)]	Nom. charge current [mA][2)]	Nom. discharge current [mA][3)]	Max. deviation to typ. values
0000_B	1.0	1.0	+/- 60%
0001_B	2.0	2.8	+/- 60 %
0010_B	4.5	5.7	+/- 60 %
0011_B	8.0	9.4	+/- 38 %
0100_B	12.5	14.2	+/- 38 %
0101_B	17.8	19.7	+/- 38 %

Table 10 Static charge and discharge currents

ICHGSTx[3:0][1]	Nom. charge current [mA][2]	Nom. discharge current [mA][3]	Max. deviation to typ. values
0110_B	23.9	26.0	+/- 38 %
0111_B	30.0	32.0	+/- 28 %
1000_B	37.1	39.5	+/- 28 %
1001_B	44.3	46.8	+/- 28 %
1010_B	52.3	54.7	+/- 28 %
1011_B	60.2	62.5	+/- 28 %
1100_B	68.3	70.6	+/- 28 %
1101_B	76.8	78.5	+/- 28 %
1110_B	86.0	87.0	+/- 28 %
1111_B	96.0	95.0	+/- 25 %

1) Refer to **ST_ICHG**
2) $V_S \geq 8V$ and $V_{GS} \leq V_{GS(ON)1}$ if ICHGSTx $\leq 7_D$, $V_S \geq 8V$ and $V_{GS} \leq V_{GS(ON)2}$ if ICHGSTx $\geq 8_D$
3) $V_{GS} \geq V_{GS(OFF)1}$ if ICHGSTx $\leq 7_D$, $V_{GS} \geq V_{GS(OFF)2}$ if ICHGSTx $\geq 8_D$

IHOLD is the hold current used to keep the gate of the external MOSFETs in the desired state. This parameter is configurable with the **IHOLD** control bit in **GENCTRL2**.

If **IHOLD** = 0:

- the MOSFETs are kept ON with the current I_{CHG8} (12.5 mA typ.)
- the MOSFETs are kept OFF with the current I_{DCHG8} (14.2 mA typ.)

If **IHOLD** = 1:

- the MOSFETs are kept ON with the current I_{CHG12} (23.9 mA typ.)
- the MOSFETs are kept with the current I_{DCHG12} (26.0 mA typ.)

The static discharge current is applied to turn off the MOSFETs when the bridge driver is in active mode when the following failures occur:

- V_S undervoltage/overvoltage
- Overtemperature
- V_{DS} overvoltage
- Charge pump undervoltage
- Overcurrent if OCEN = 1

6.2.1 Static activation of a high-side MOSFET

Turn-on with cross-current protection

If LSx is ON (HBxMODE[1:0] = 01_B), before the activation of HSx (HBxMODE[1:0] = 10_B) then the high-side MOSFET is turned on after a cross-current protection time (refer to **Figure 7**):

- after the CSN rising edge and for the duration $t_{HBxCCP\ Active}$:
  - the high-side MOSFET is kept OFF with the current -ICHGSTx
  - the gate of the low-side MOSFET is discharged with the current -ICHGSTx

- at the end of $t_{HBxCCP\ Active}$ and for the duration $t_{HBxBLANK\ Active} + t_{FVDS}$:
  - the gate of the high-side MOSFET is charged with the current ICHGSTx
  - low-side MOSFET is kept OFF with the current -IHARDOFF (hard off phase)
- at the end of t_{FVDS}:
  - the drive current of the high-side MOSFET is reduced to IHOLD
  - the drive current of the low-side MOSFET is set to -IHOLD

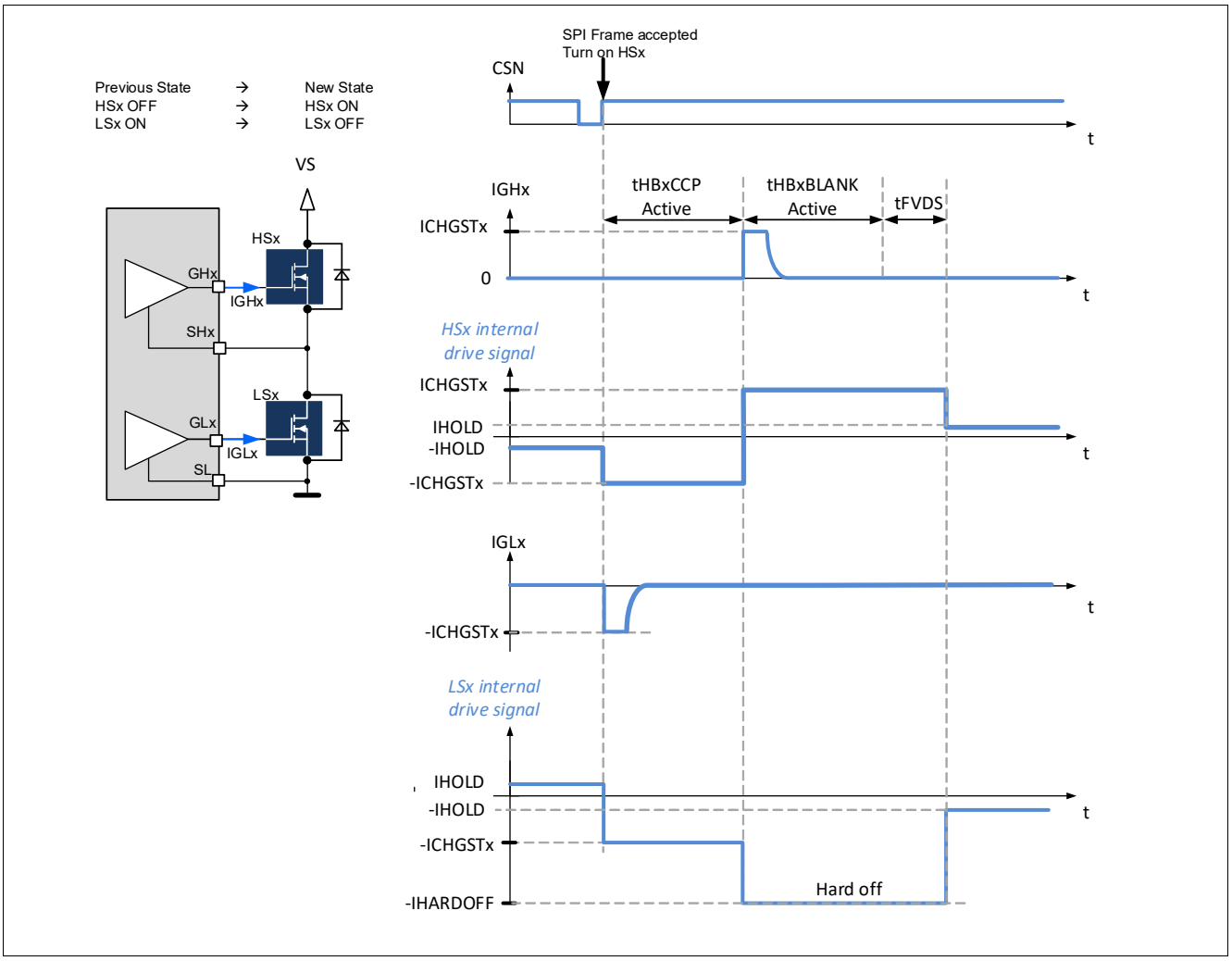


Figure 7 Turn-on of a high-side MOSFET with cross-current protection

Note: The CSN rising edge must be synchronized with the device logic. Therefore SPI commands are executed with a delay of up to 3 µs after the CSN rising edge.

Turn-on without cross-current protection

If LSx is OFF (HBxMODE[1:0] = 00_B), before the activation of HSx (HBxMODE[1:0] = 10_B), then the high-side MOSFET is turned on without cross-current protection (refer to **Figure 8**):

- after the CSN rising edge and for a duration $t_{HBxBLANK\ Active} + t_{FVDS}$:
  - the gate of the high-side MOSFET is charged with the current ICHGSTx
  - the low-side MOSFET is kept OFF with the current -IHARDOFF
- at the end of t_{FVDS}:
  - the drive current of the high-side MOSFET is reduced to IHOLD
  - the drive current of the low-side MOSFET is set to -IHOLD

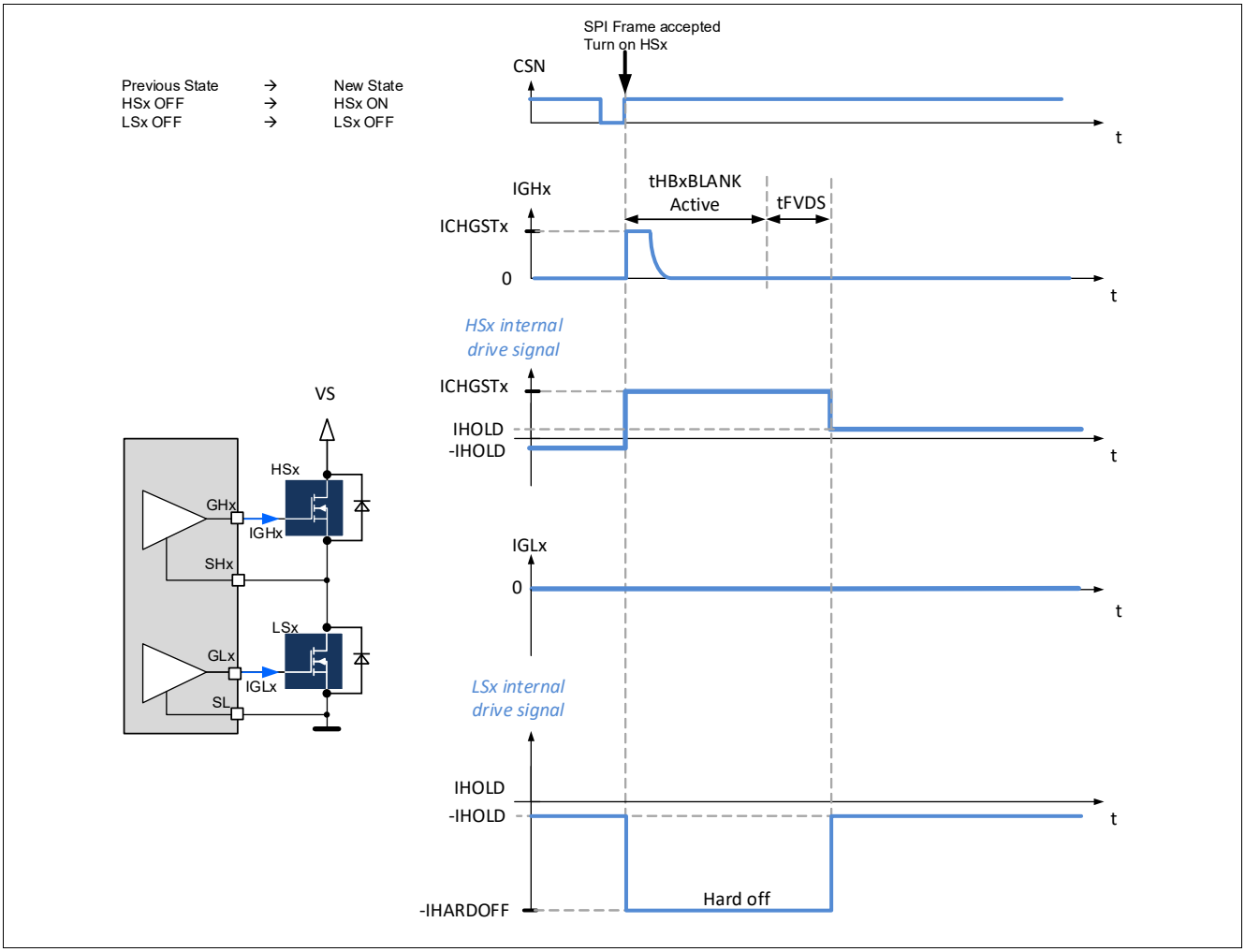


Figure 8 Turn-on of a high-side MOSFET without cross-current protection

Note: The CSN rising edge must be synchronized with the device logic. Therefore SPI commands are executed with a delay of up to 3 µs after the CSN rising edge.

6.2.2 Static activation of a low-side MOSFET

The description of the static activation of a low-side x differs from the description of **Chapter 6.2.1** only by exchanging high-side x and low-side x.

6.2.3 Turn-off of the high-side and low-side MOSFETs of a half-bridge

When the TLE92104-232 receives a SPI to turn-off both the high-side and low-side MOSFETs of the half-bridge x (HBxMODE[1:0] = (0,0) or (1,1)):

- the gate of HSx and LSx are discharged with the current -ICHGSTx for the duration $t_{HBxCCP\ Active}$ (**Figure 9**)
- at the end of $t_{HBxCCP\ Active}$, the drive current of HSx and LSx are reduced to -IHOLD

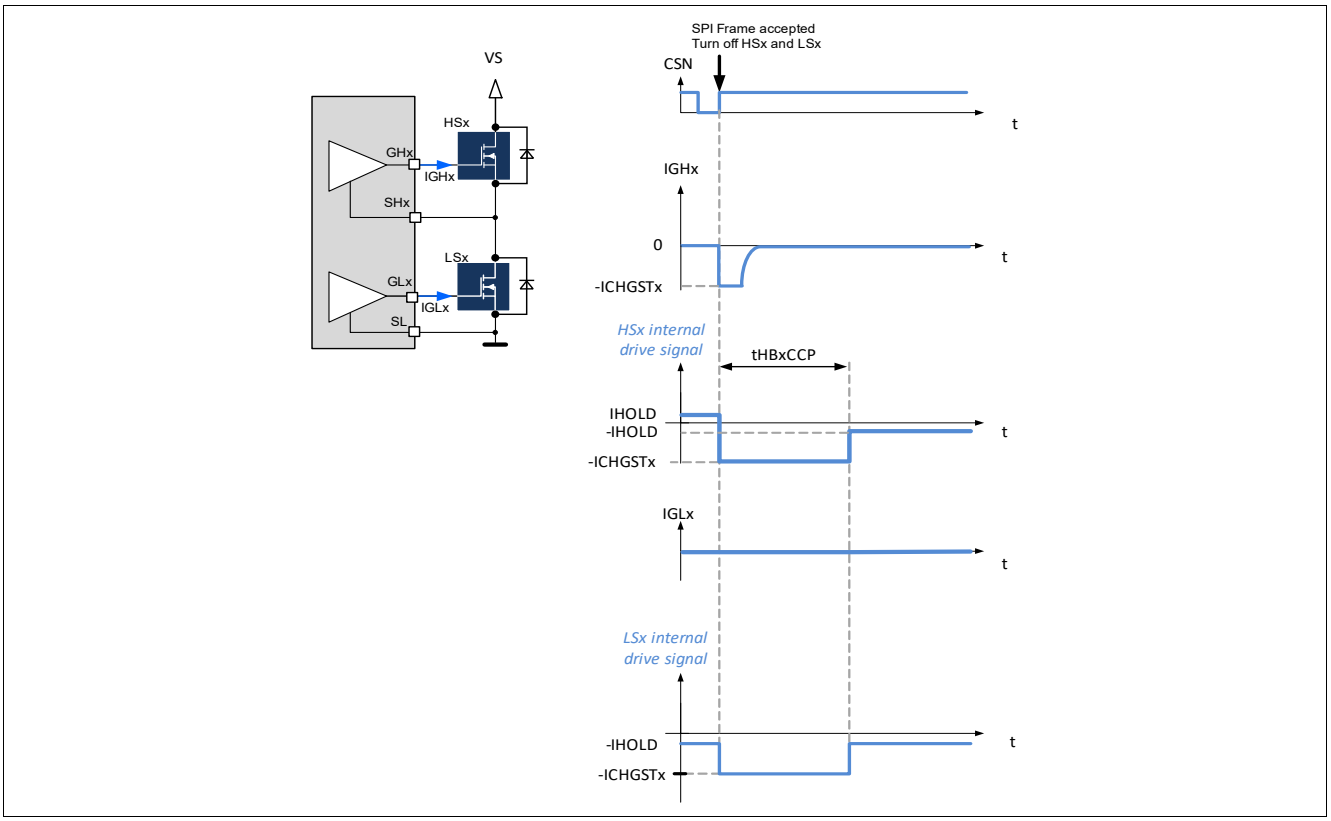


Figure 9 Turn-off of the high-side and low-side MOSFETs of a half-bridge

Note: The CSN rising edge must be synchronized with the device logic. Therefore SPI commands are executed with a delay of up to 3 µs after the CSN rising edge.

6.3 PWM operation with bridge driver in active mode (BD_PASS = 0)

The TLE92104-232 integrates three PWM channels. The pins PWM1,PWM2 and PWM3 provide the PWM signal for each PWM channel.

One half-bridge can be mapped to one of the PWM channels according the settings of the control registers **HBMODE** and **PWMSET** (see **Table 11**):

- PWMxEN in **PWMSET**, enables or disables the PWM channel x
- The control bits PWMx_HB[2:0] in **PWMSET** select the half-bridge
- The control bits HBMODE[1:0] (**HBMODE**) of the half-bridge selected by PWMx_HB[2:0] configures the low-side or the high-side MOSFET in PWM mode

Example: the following bits must be set to map the low-side of HB3 to the PWM channel 2 (start sequence with PWM):

1. Set HB3MODE[1:0] to (0,0): HB3 is in high impedance
2. Set PWM2HB[2:0] to (x,1,0) and set PWM2EN to 1 (HB3 stays in high impedance, independently from the signal present at the PWM2 pin)
3. Set HB3MODE[1:0] to (0,1): PWM2 is applied to the low-side of HB3

Table 11 PWM channel settings

PWMxEN[1)]	PWMx_HB[2:0] [1)]	HByMODE[1:0][2)]	PWMx channel setting[1)]
0_B	don't care	don't care	no PWM operation
don't care$_B$	don't care$_B$	00_B	no PWM operation on the selected HB
don't care$_B$	don't care$_B$	11_B	no PWM operation on the selection HB
1_B	000_B or 100_B	01_B	Low-side of HB1 is mapped to PWMx
1_B	001_B or 101_B	01_B	Low-side of HB2 is mapped to PWMx
1_B	010_Bor 110_B	01_B	Low-side of HB3 is mapped to PWMx
1_B	011_B or 111_B	01_B	Low-side of HB4 is mapped to PWMx
1_B	000_B or 100_B	10_B	High-side of HB1 is mapped to PWMx
1_B	001_B or 101_B	10_B	High-side of HB2 is mapped to PWMx
1_B	010_Bor 110_B	10_B	High-side of HB3 is mapped to PWMx
1_B	011_B or 111_B	10_B	High-side of HB4 is mapped to PWMx

1) x = 1 ... 3.

2) the half-bridge y is selected by the PWMx_HB[2:0] bits.

*Note: An SPI error is reported if one half-bridge is mapped to several activated PWM channels. In this case the external MOSFETs of the impacted half-bridge are turned-off and the corresponding status bit (HBxPWME) of the **HBVOUT_PWMERR** register is set.*

6.3.1 Determination of the active and free-wheeling MOSFET

An active free-wheeling is automatically implemented when a half-bridge is activated in PWM mode to reduce the power dissipation of the free-wheeling (FW) MOSFET: If the active MOSFET is OFF, the opposite (free-wheeling) MOSFET of the same half-bridge is actively turned on. See **Figure 11**, **Figure 12**, **Figure 13**, **Figure 14**, .

If **EN_GEN_CHECK** = 0: the PWM MOSFET is considered as the active MOSFET and the opposite MOSFET of the same half-bridge is considered as the free-wheeling MOSFET.

If **EN_GEN_CHECK** = 1: At the end of the cross-current protection times (tHBxCCP Active, tHBxCCP FW) of each MOSFET (both MOSFETs are supposed to be off) the device detects which MOSFET of the half-bridge is the active MOSFET and which MOSFET is the FW MOSFET (**Figure 10**).

- If VSHx > **V_{SHH}**: The high-side MOSFET is the FW MOSFET and the low-side MOSFET is the active MOSFET
- If VSHx < **V_{SHL}**: Then the low-side MOSFET is the FW MOSFET and the high-side MOSFET is the active MOSFET
- If **V_{SHL}** < VSHx < **V_{SHH}**: No clear distinction between the FW MOSFET and the active MOSFET. The MOSFET to be turned on is considered as the active MOSFET.

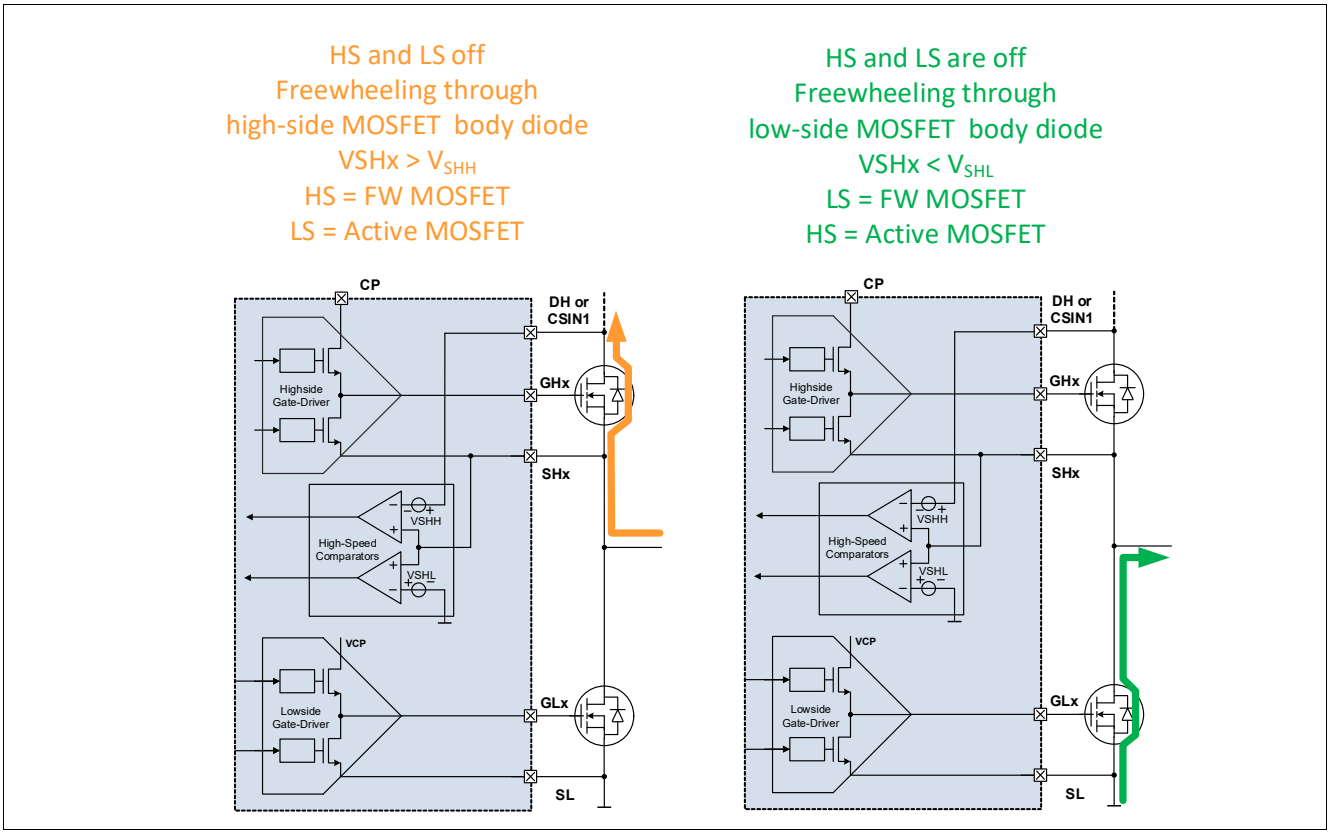


Figure 10 Detection principle of the active and freewheeling MOSFET

Note: The PWM signal is applied to the MOSFET selected by HBxMODE[1:0], independently from the free-wheeling and the active MOSFET.

*Note: It is not possible to determine the active or FW MOSFET if the PWM on-time is shorter than tHBxCCP FW, or if the PWM-off-time is shorter than tHBxCCP Active (Refer to **Chapter 6.3.5**). In this case, the PWM MOSFET is considered as the active MOSFET. In other words, it is assumed that the motor operates as load.*

Figure 11, **Figure 12** show examples of free-wheeling and active MOSFET when the motor operates as load.

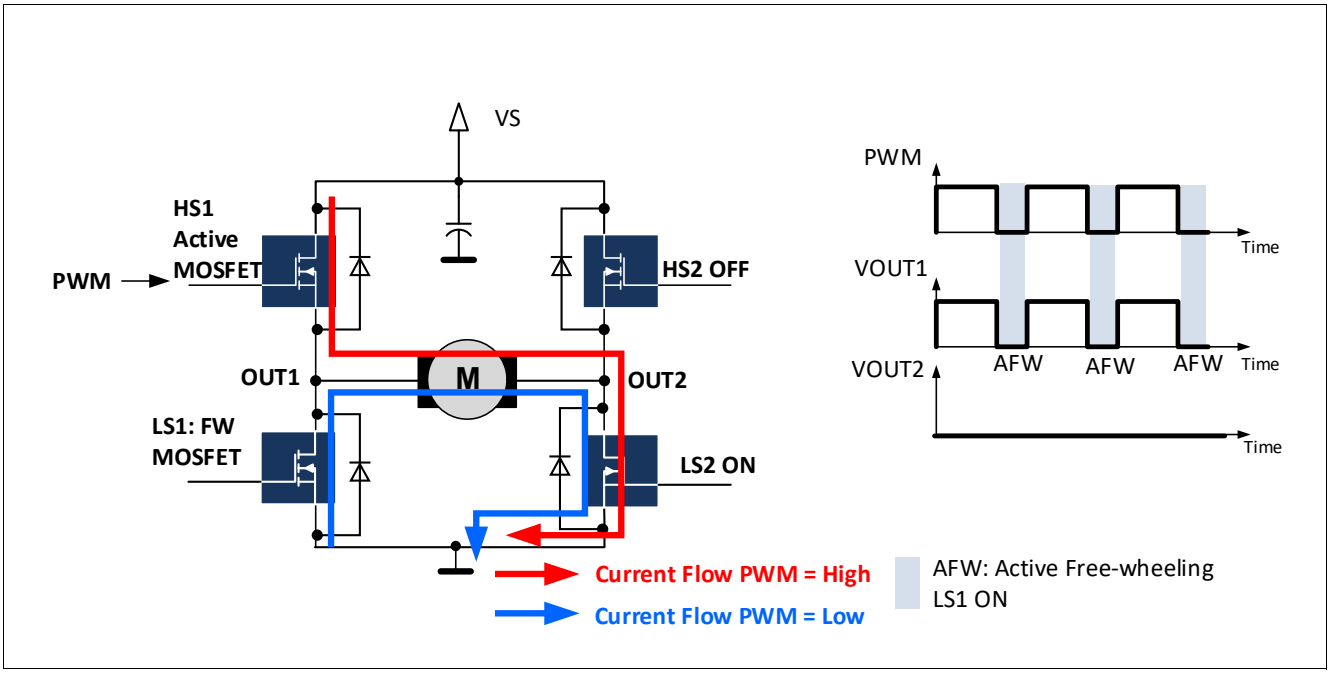


Figure 11 Active freewheeling on HB1: PWM1EN = 1. PWM applied to HS1 (HB1MODE[1:0] = 10_B). The motor operates as load: HS1 is the active MOSFET, LS1 is the FW MOSFET.

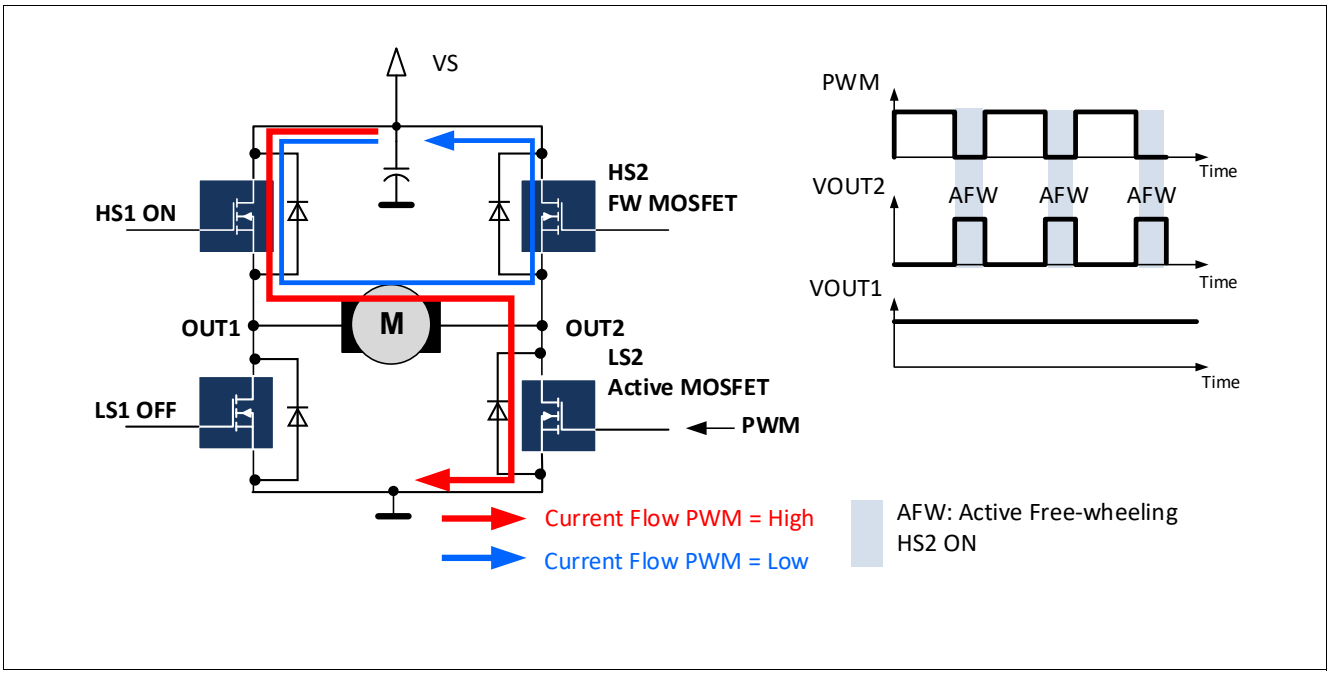


Figure 12 Active freewheeling on HB2: PWM1EN = 1. PWM applied to LS2 (HB2MODE[1:0] = 01_B). The motor operates as load: LS2 is the active MOSFET, HS2 is the FW MOSFET.

Figure 13 and **Figure 14** show examples of free-wheeling and active MOSFET when the motor operates as generator.

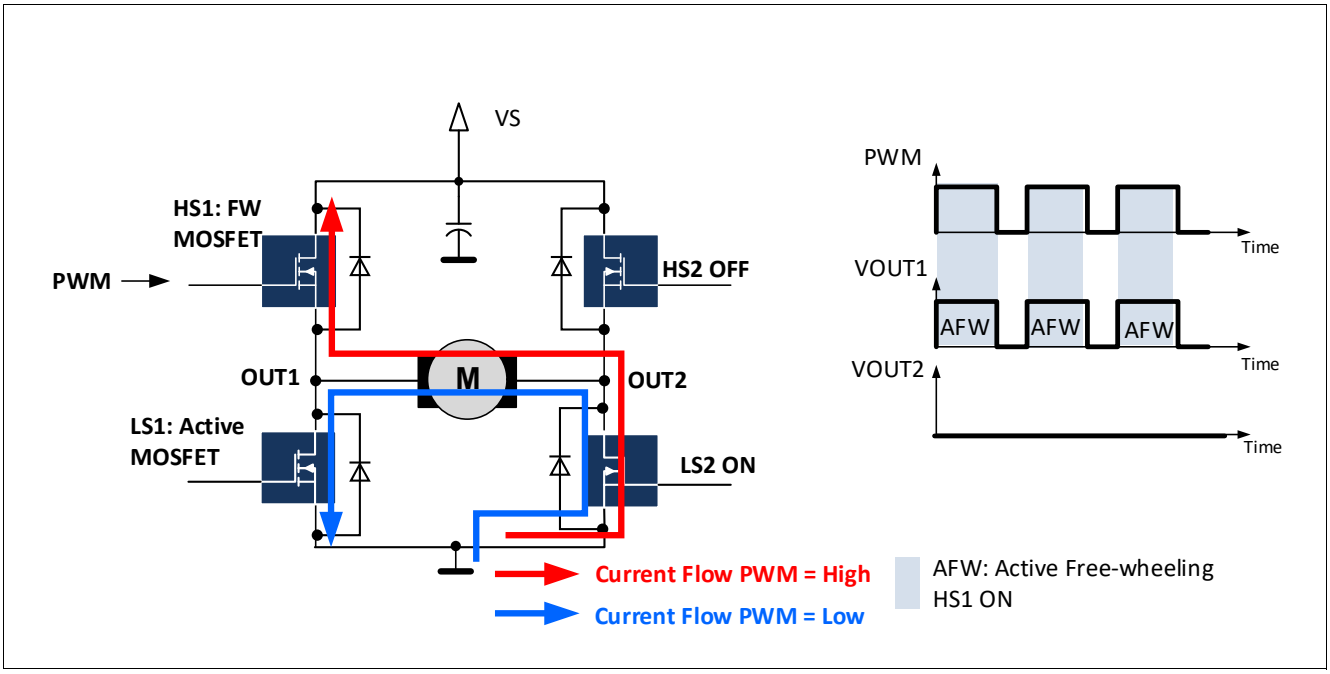


Figure 13 Active freewheeling on HB1: PWM1EN = 1. PWM applied to HS1 (HB1MODE[1:0] = 10_B).The motor operates as generator: LS1 is the active MOSFET, HS1 is the FW MOSFET.

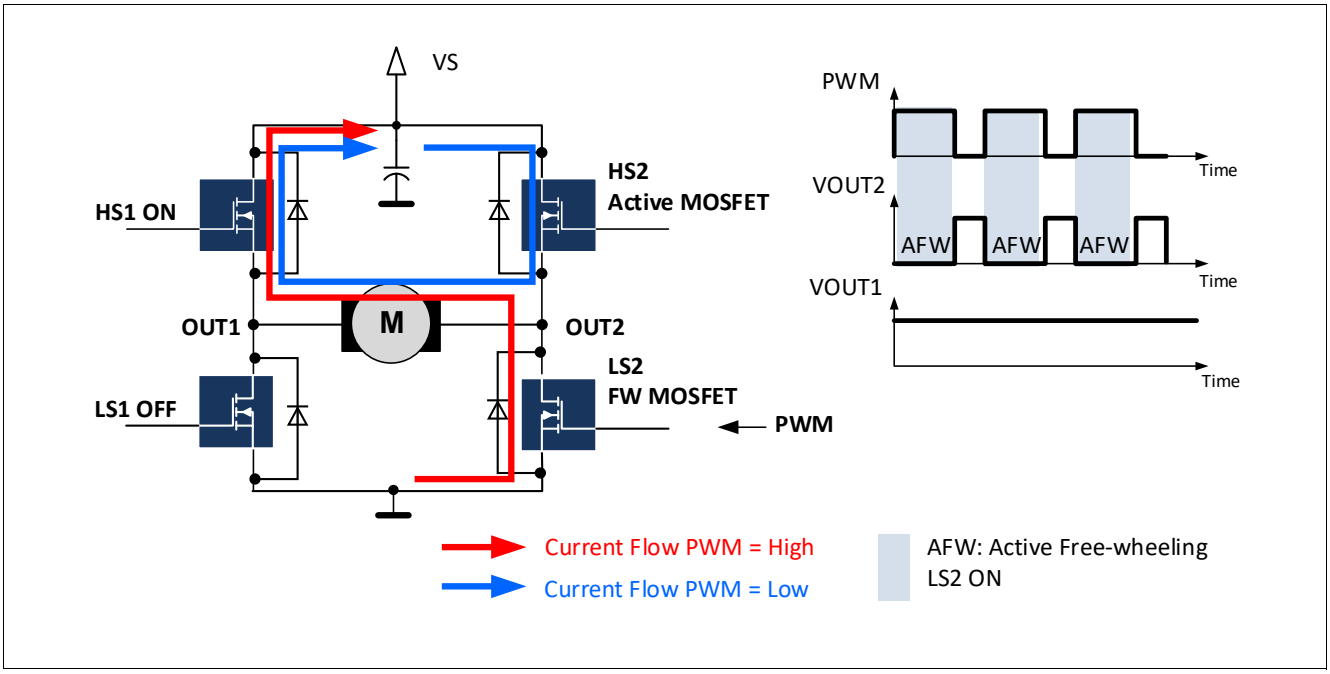


Figure 14 Active freewheeling on HB2: PWM1EN = 1. PWM applied to LS2 (HB2MODE[1:0] = 01_B). The motor operates as generator: HS2 is the active MOSFET, LS2 is the FW MOSFET.

6.3.2 Configuration in PWM mode

The following sections describe the different control schemes in PWM mode. They differ during the pre-charge and pre-discharge phases (**Figure 15**):

- Adaptive gate control (AGC[1:0] = (1,0) or (1,1), **GENCTRL2**): in this mode a pre-charge current and a pre-discharge current are applied to the gate of the PWM MOSFET. These currents are used to regulate the effective turn-on and turn-off delays to the respective target values. Refer to **Chapter 6.3.3**.

Floating gate drivers

- No adaptive gate control (AGC[1;0] = (0,0)): in this mode, the pre-charge and pre-discharge phases are deactivated. Refer to **Chapter 6.3.4.1**.
- No adaptive gate control (AGC[1;0] = (0,1)). In this mode:
  - the pre-charge phase is deactivated
  - during the pre-discharge phase, the gate of the PWM MOSFET mapped to the PWM channel x, x = 1…3, is discharged with the configured current IPCHGINIT (Refer to **PWM_PCHG_INIT** and **Chapter 6.3.4.2**)

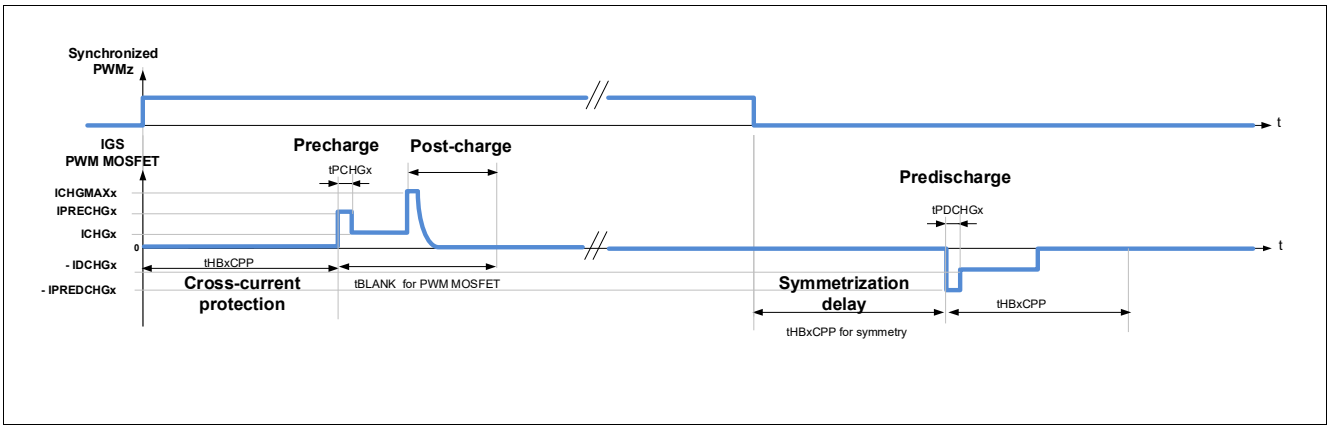


Figure 15 PWM overview showing pre-charge, pre-discharge and post charge phases, AGC[1:0] = 10_B or 11_B, POCHGDIS = 1_B.

6.3.3 PWM operation with adaptive gate control

This section describes the MOSFETs control during high-side or low-side PWM operation when the adaptive gate control is enabled (AGC[1:0] = (1,0) or (1,1), **GENCTRL2**).

Refer to **Chapter 6.3.1** for the definition of the active and of the freewheeling MOSFET according to the setting of **AGC**.

Assumption: a high-side or low-side MOSFET driver is mapped to the PWM channel z, z = 1,2 or 3.

Refer to **Figure 16** for high-side PWM and **Figure 19** for low-side PWM for the description of the switching phase.

The TLE92104-232 adapts the pre-charge current, respectively the pre-discharge current, in order to match the effective turn-on delay (t_{DON}) and turn-off delay (t_{DOFF}) to the configured values.

The configured turn-on and turn-off delays of the respective PWM MOSFETs are set by the registers **TDON_OFF1**, **TDON_OFF2**, **TDON_OFF3**.

The effective turn-on and turn-off delays of the respective active MOSFETs are read out from the status registers **EFF_TDON_OFF1**, **EFF_TDON_OFF2**, **EFF_TDON_OFF3**.

Table 12 Abbreviations for adaptive turn-on and turn-off phases in PWM configuration

Abbreviation	Definition
Suffix x	Related to the half-bridge x (x = 1 … 4)
Suffix z	Related to the PWM channel z (z = 1,2 or 3)
VGS_HSx	Gate-Source voltage of high-side MOSFET x
IGS_HSx	Gate current of high-side MOSFET x IGS_HSx is positive when the current flows out of GHx.
VGS_LSx	Gate-Source voltage of low-side MOSFET x
IGS_LSx	Gate current of low-side MOSFET x IGS_LSx is positive when the current flows out of GLx.
tHBxCCP ACTIVE	Active cross-current protection time of HBx. See control registers **CCP_BLK1**, **CCP_BLK2_ACT**, **PWM_ICHGMAX_CCP_BLK3_ACT** and **Chapter 7.5**.
tHBxBLANK ACTIVE	Active Drain-source overvoltage blank time of HBx. See control registers **CCP_BLK1**, **CCP_BLK2_ACT**, **PWM_ICHGMAX_CCP_BLK3_ACT** and **Chapter 7.5**.
tHBxCCP FW	Freewheeling cross-current protection time of HBx. See control registers **CCP_BLK1**, **CCP_BLK2_FW**, **PWM_ICHGMAX_CCP_BLK3_FW** and **Chapter 7.5**
tHBxBLANK FW	Freewheeling drain-source overvoltage blank time of HBx. See control registers **CCP_BLK1**, **CCP_BLK2_FW**, **PWM_ICHGMAX_CCP_BLK3_FW** and **Chapter 7.5**
PWMz	External PWM signal applied to the input pin PWMz.
ICHGMAXz	Maximum drive current of the half-bridge mapped to PWM channel z during the pre-charge and pre-discharge phases. See control registers **PWM_ICHGMAX_CCP_BLK3_ACT** and **PWM_ICHGMAX_CCP_BLK3_FW** ICHGMAXz is also the drive current for the post-charge phase IPRECHGz and IPREDCHGz are limited to ICHGMAXz.

Table 12 Abbreviations for adaptive turn-on and turn-off phases in PWM configuration

Abbreviation	Definition
IPRECHGz	Pre-charge current sourced by the gate driver mapped to the PWM channel z during tPCHGz. Internal and self-adaptive parameter (if **AGC** = (1,0) or (1,1), **GENCTRL2**) IPRECHGz is clamped between I_{CHG0} and ICHGMAXz.
IPCHGINITz	Initial value of IPRECHGz. Refer to **PWM_PCHG_INIT**
IPREDCHGz	Pre-discharge-current sunk by the gate driver mapped to the PWM channel z during tPDCHGz. Internal and self-adaptive parameter. (**AGC** = (1,0) or (1,1), **GENCTRL2**) IPREDCHGz is clamped between I_{DCHG0} and IDCHGMAXz.
IPDCHGINITz	Initial value of IPREDCHGz. Refer to **PWM_PDCHG_INIT**
ICHGz	Current sourced by the gate driver mapped to the PWM channel z during the charge phase. See control register **PWM_ICHG_ACT**.
IDCHGz	Current sunk by the gate driver mapped to the PWM channel z during the discharge phase. See control register **PWM_IDCHG_ACT**.
ICHGFWz	Current source or sunk by the gate driver to turn on / turn off the freewheeling MOSFET of the half-bridge mapped to the PWM channel z. See **PWM_ICHG_ACT**.
tPCHGz	Duration of the pre-charge phase of PWM channel z. tPCHGz is configurable by SPI. See control register **TPRECHG**, configuration bits TPCHGz[1:0].
tPDCHGz	Duration of the pre-discharge phase of PWM channel z. tPDCHGz is configurable by SPI. See control register **TPRECHG**, configuration bits TPDCHGz[1:0].
tDONz	Turn-on delay of the PWM MOSFET mapped to the PWM channel z: • for high-side PWM: time between the end of the cross-current protection and when VSHx increases to V_{SHL} (**Figure 17**). • for low-side PWM: time between the end of the cross-current protection and when VSHx decreases to V_{SHH}.
tDOFFz	Turn-off delay of the PWM MOSFET mapped to the PWM channel z: • for high-side PWM: time between the end of the symmetrization delay (t_{HBxCCP}) and when VSHx decreases to **V_{SHH}** (**Figure 18**). • for low-side PWM: time between the end of the symmetrization delay (t_{HBxCCP}) and when VSHx increases to **V_{SHL}**.
IHOLD	Hold current sourced or sunk by the gate driver to keep the MOSFET in the desired state. See IHOLD control bit in **GENCTRL2**.
IHARDOFF	IHARDOFF is the maximum current that the gate drivers can sink. It corresponds to the discharge current when IDCHGx[4:0] = 31_D (100 mA typ.).
TFVDS	Drain-Source overvoltage filter time. See **GENCTRL2**.

6.3.3.1 High-side PWM with adaptive gate control, motor operating as load

The following section describes the MOSFET control when the PWM signal is applied to the high-side MOSFET of one half-bridge while the motor operates .

Assumption: the PWM channel z, z = 1,2 or 3, is applied to the high-side MOSFET of the half-bridge x, x = 1 … 4.

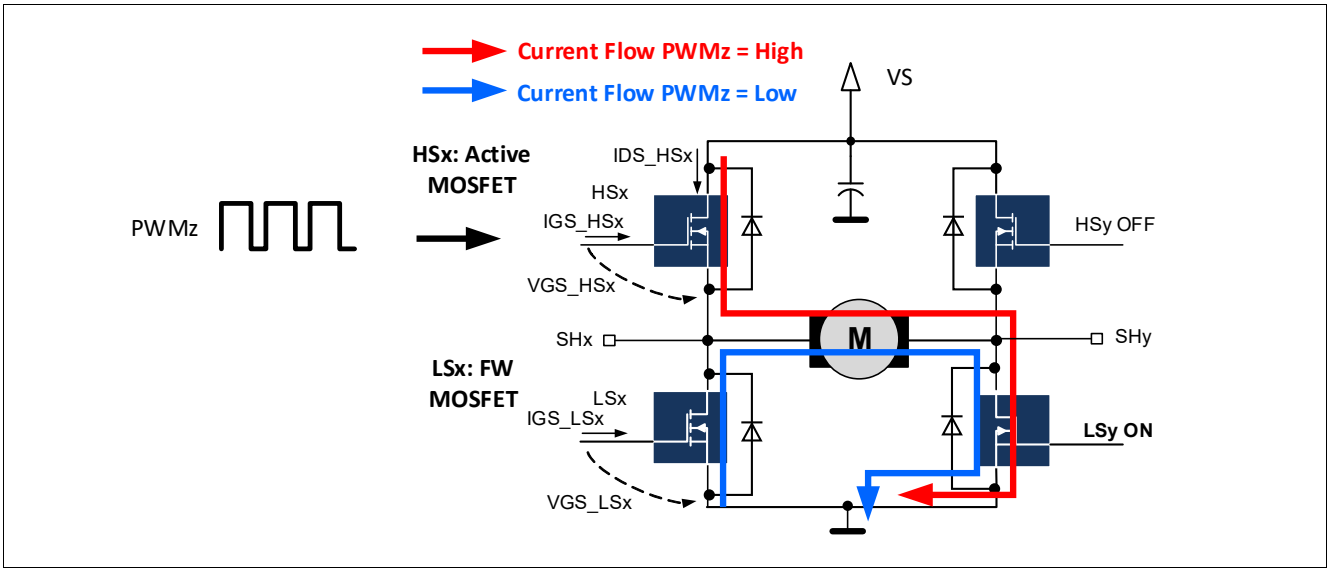


Figure 16 PWM channel z is mapped to high-side x, motor operating as load

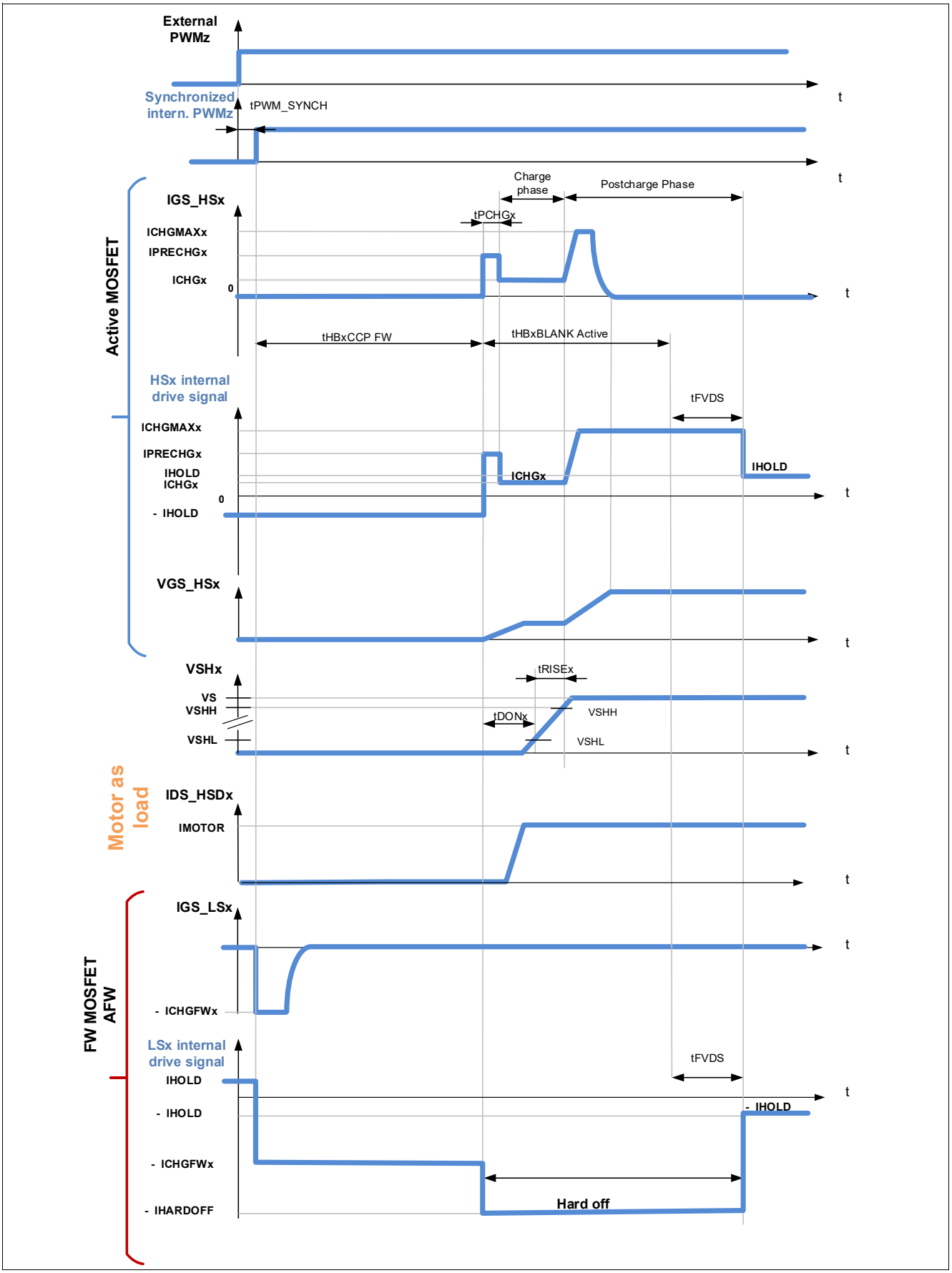


Figure 17 Adaptive turn-on, high-side PWM, AGC[1:0] = (1,0) or (1,1), motor operating as load

Floating gate drivers

Adaptive turn-on during high-side PWM

The turn-on of the high-side MOSFET is done in four phases (Refer to **Figure 17**):

1. **Cross-current protection phase**: The cross-current protection tHBxCCP FW starts at the rising edge of the internal PWMz signal[1]. During tHBxCCP FW, the low-side MOSFET x is turned off with the discharge current - ICHGFWx, while the high-side MOSFET x is kept off. .
2. **Pre-charge:** Once tHBxCCP FW has elapsed, the gate of the high-side MOSFET x is pre-charged with the current IPRECHGz for a duration tPCHGz. IPRECHGz[2] is an internal parameter, which is self-adaptive (see next phase).
3. **Charge:** After tPCHGz, the charge current is decreased from IPRECHGz down to ICHGz. The effective tDONz[3] is measured and compared to the configured tDONz for the automatic adaptation of IPRECHGz (see **Adaptive control of pre-charge current**). The charge phase ends up when V_{SHx} reaches V_{SHH}.
4. **Post-charge:** After the charge phase, the control signal for the charge current of HSx is increased by one current step every 62.5 ns typ. to ICHGMAXx.

*Note: The postcharge phase is deactivated by setting **POCHGDIS** to 1. Refer to **GENCTRL2**.*

Adaptive control of pre-charge current

Refer to **Chapter 6.3.6** for information on the pre-discharge currents.

The pre-charge current IPRECHGz is a self-adaptive parameter if AGC[1:0] = (1,0) or (1,1) (see **GENCTRL2**). It is applied during tPCHGz (see **TPRECHG**). The TLE92104-232 adapts IPRECHGz to match the effective tDONz to the configured value.

IPRECHGz is clamped between I_{CHG0} (1 mA typ.) and ICHGMAXz (see **PWM_ICHGMAX_CCP_BLK3_ACT**).

IPRECHGz is initialized to min(IPCHGINITz, ICHGMAXz) (refer to **PWM_PCHG_INIT**) when the TLE92104-232 receives an SPI command setting PWMz_EN to 1 (see **PWMSET**).

The following adaptive schemes can be selected:

AGCFILT = 0 (**GENCTRL2**): No filter is applied

- If the effective tDONz is longer than the configured tDONz, then IPRECHGz is increased during the next pre-charge phase.
- If the effective tDONz is shorter than the configured tDONz, then IPRECHGz is decreased during the next pre-charge phase.
- The pre-charge current is increased or decreased by one, respectively by two current steps (**Chapter 6.3.6**) if the control bit IPCHGADT in the control register **GENCTRL1** is set to 0 respectively 1.

AGCFILT = 1: The filter is applied

- If the effective tDONz **of the last two PWM cycles** are longer than the configured tDONz, then IPRECHGz is increased during the next pre-charge phase.

1) The external PWMz signal is synchronized with the internal device clock, resulting in the delay t_{PWM_SYNCH} between the internal and the external PWMz signals.
2) IPRECHGz is clamped between ICHGMAXz and I_{CHG0}.
3) The effective tDON can be read out. Refer to **EFF_TDON_OFF1**,**EFF_TDON_OFF2**, **EFF_TDON_OFF3**

- If the effective tDONz **of the last two PWM cycles** are shorter than the configured tDONz, then IPRECHGz is decreased during the next pre-charge phase.
- The pre-charge current is increased or decreased by one, respectively by two current steps (**Chapter 6.3.6**) if the control bit IPCHGADT in the control register **GENCTRL1** is set to 0 respectively 1.
- If none of the two cases are applicable, then IPRECHGz is unchanged during the next pre-charge phase.

Floating gate drivers

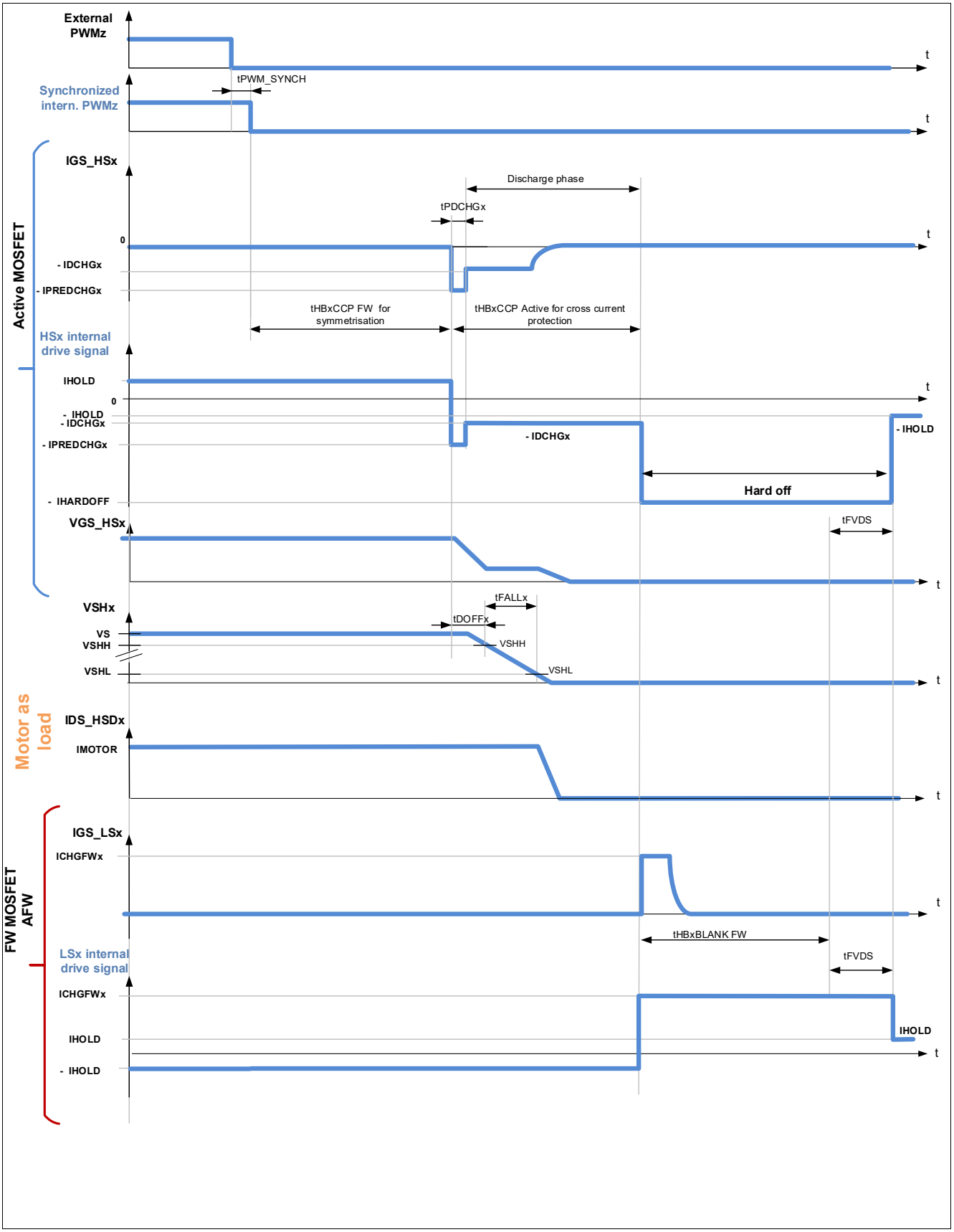


Figure 18 Adaptive turn-off, high-side PWM, AGC[1:0] = (1,0) or (1,1), motor operating as load

Adaptive turn-off during high-side PWM

Floating gate drivers

The turn-off of the high-side MOSFET is done in four phases (Refer to **Figure 18**):

1. **Turn-off delay time for symmetrization** of the PWM signal: The turn-off of HSx is delayed by tHBxCCP FW after the falling edge of the internal PWMz signal[1], in order to compensate the distortion caused by the cross-current protection time at turn-on.
2. **Pre-discharge:** once tHBxCCP FW for symmetrization has elapsed, the gate of the high-side MOSFET x is pre-discharged with the current - IPREDCHGz for a duration tDPCHGz. IPREDCHGz is a device internal parameter, which is self-adaptive (See next phase).
3. **Discharge:** After tPREDCHGz, the pre-discharge current is decreased in absolute value from IPREDCHGz[2] down to IDCHGz. The effective tDOFF[3] is measured and compared to the configured tDOFFz for the automatic adaptation of IPREDCHGz (see **Adaptive control of pre-discharge current**). The discharge phase ends up at expiration of tHBxCCP active for cross-current protection.
4. **Cross-current protection phase:** The cross-current protection is concurrent to the pre-discharge and discharge of the high-side MOSFET. The cross-current protection phase starts when the turn-off delay for symmetrization ends up. It has the duration tHBxCCP active. During tHBxCCP active, the low-side MOSFETx is kept OFF. When tHBxCCP active has elapsed, the gate of the low-side MOSFET x is charged with the current ICHGFWz until the end of tFVDS, provided that $V_{SHx} < V_{SHL}$.

Adaptive control of pre-discharge current

Refer to **Chapter 6.3.6** for information on the pre-discharge currents.

The pre-discharge current IPREDCHGz is a self-adaptive parameter if AGC[1:0] = (1,0) or (1,1) (see **GENCTRL2**). The TLE92104-232 adapts the IPREDCHGz to match the measured t_{DOFFz} to the configured value.

IPREDCHGz is clamped between I_{DCHG0} (1 mA typ.) and ICHGMAXz (see **PWM_ICHGMAX_CCP_BLK3_ACT**).

IPREDCHGz is initialized to min(IPDCHGINITz, ICHGMAXz) (refer to **PWM_PDCHG_INIT**) when the TLE92104-232 receives a SPI command setting PWMz_EN to 1 (see **PWMSET**)

The pre-discharge current is increased or decreased by one, respectively by two current steps (**Chapter 6.3.6**) if the control bit IPCHGADT in the control register **GENCTRL1** is set to 0 respectively 1.

The following adaptive schemes can be selected:

AGCFILT = 0 (**GENCTRL2**): No filter is applied

- If the effective tDOFFz is longer than the configured tDOFFz, then IPREDCHGz is increased during the next pre-discharge phase
- If the effective tDOFFz is shorter than the configured tDOFFz, then IPREDCHGz is decreased during the next pre-discharge phase
- The pre-charge current is increased or decreased by one, respectively by two current steps (**Chapter 6.3.6**) if the control bit IPCHGADT in the control register **GENCTRL1** is set to 0 respectively 1.

AGCFILT = 1: The filter is applied

1) The external PWMz signal is synchronized with the internal device clock, resulting in the delay t_{PWM_SYNCH} between the internal and the external PWMz signals.
2) IPREDCHGz is clamped between ICHGMAXz and I_{DCHG0}.
3) The effective tDOFF can be read out. Refer to **EFF_TDON_OFF1**,**EFF_TDON_OFF2**, **EFF_TDON_OFF3**.

- If the effective tDOFFz **of the last two PWM cycles** are longer than the configured tDOFFz, then IPREDCHGz is increased during the next pre-charge phase.
- If the effective tDOFFz **of the last two PWM cycles** are shorter than the configured tDOFFz, then IPREDCHGz is decreased during the next pre-charge phase.
- If none of the two cases are applicable, then IPRECHGz is unchanged during the next pre-charge phase.
- The pre-charge current is increased or decreased by one, respectively by two current steps if the control bit IPCHGADT is set to 0 respectively 1.

6.3.3.2 Low-side PWM with adaptive gate control, motor operating as load

The following section describes the MOSFET control when the PWM signal is applied to the low-side MOSFET of one half-bridge.

Assumption: the PWM channel z, z = 1,2 or 3, is applied to the low-side MOSFET of the half-bridge x, x = 1 … 4 (**Figure 19**).

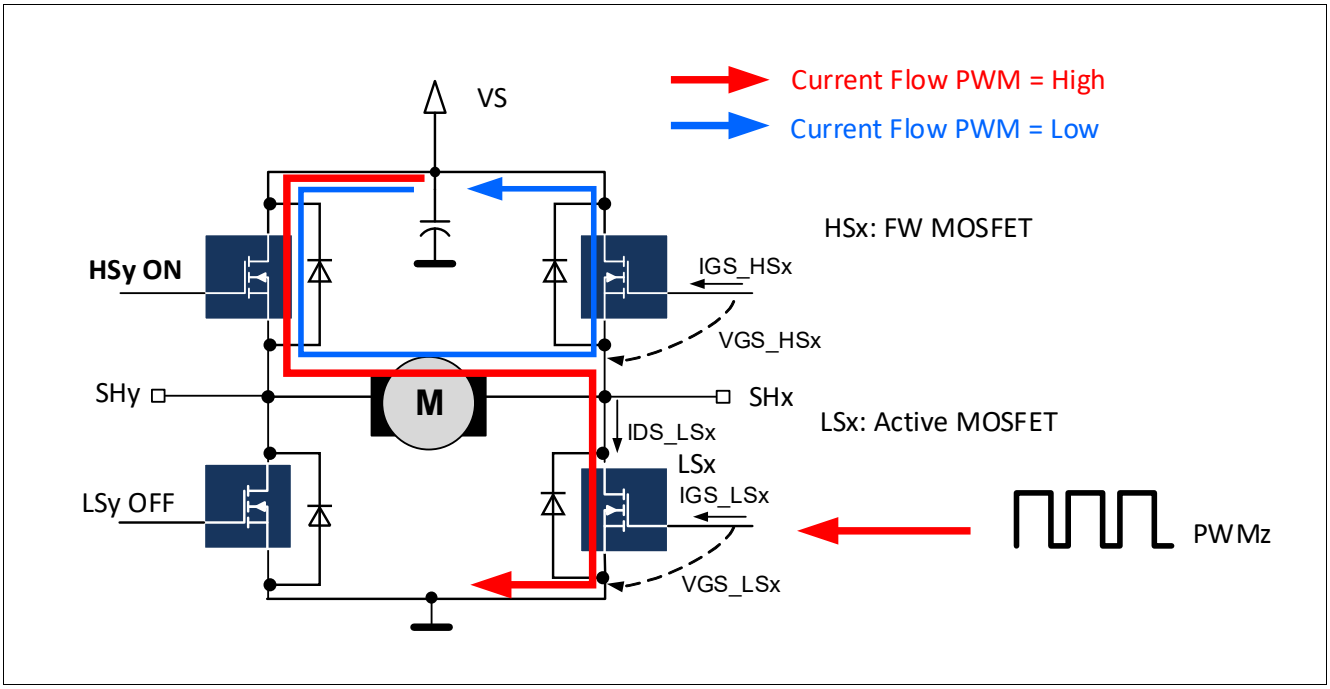


Figure 19 PWM Channel z is mapped to low-side x, motor operating as load

The description of the control of the PWM half-bridge differs from the description of **Chapter 6.3.3.1** only by exchanging high-side x and low-side x and the thresholds V_{SHH} and V_{SHL}.

6.3.3.3 High-side PWM with adaptive gate control, motor operating as generator

The control scheme during high-side PWM in generator mode (refer to **Figure 20**) is equivalent to low-side MOSFET in load mode with the complementary signal of the external PWM input.

The turn-on, turn-off delay times and the rise and fall times are applied and measured for the active MOSFET.

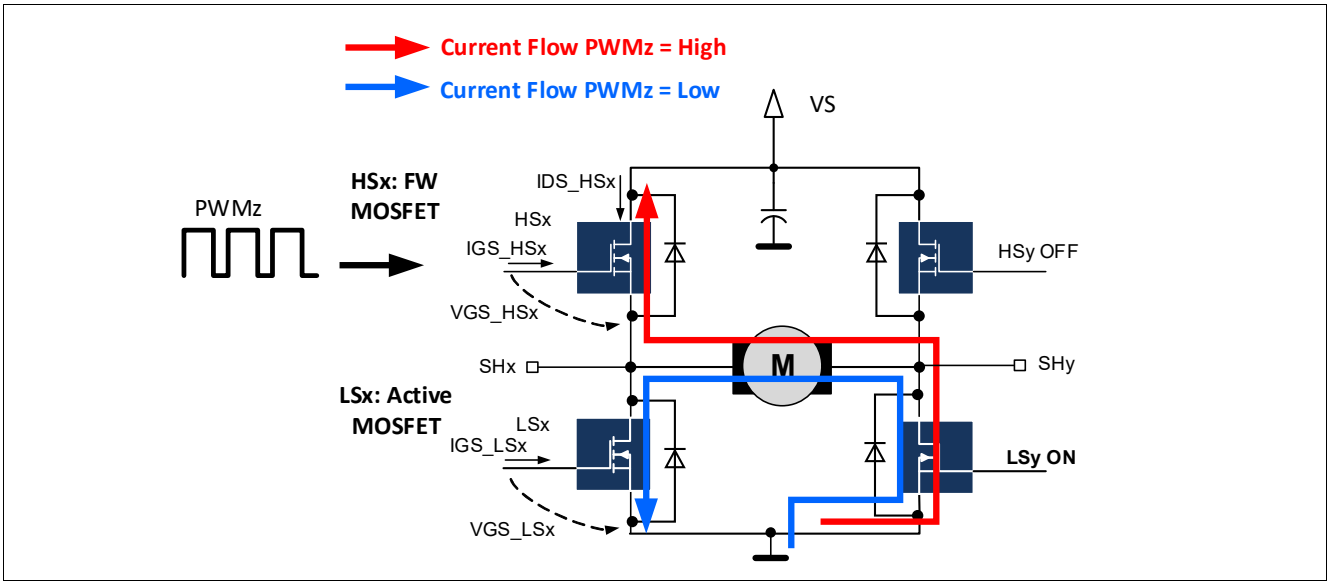


Figure 20 PWM input z is mapped to high-side x, the motor operating as generator

Floating gate drivers

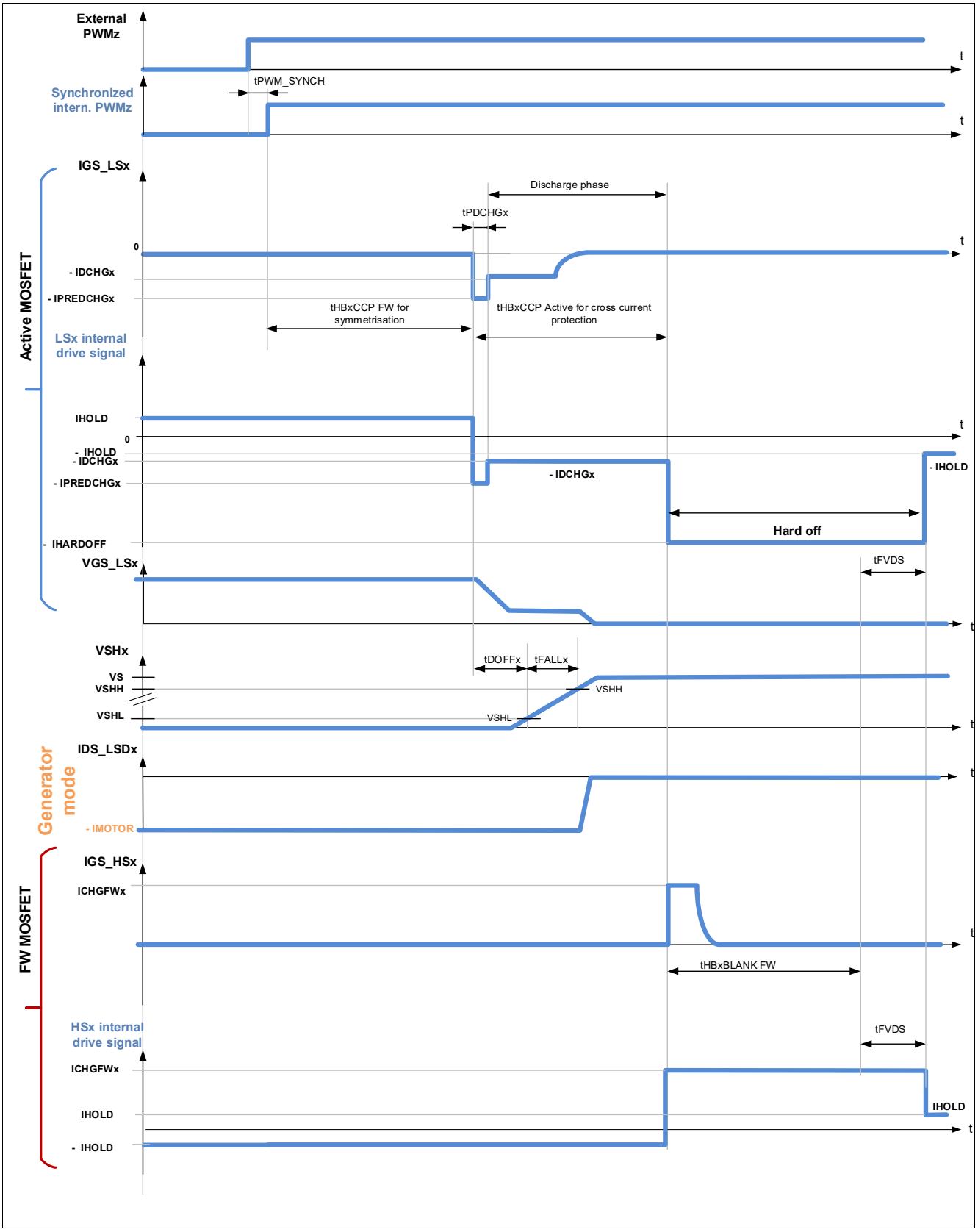


Figure 21 Adaptive turn-on, high-side PWM, AGC[1:0] = (1,0) or (1,1), motor operating as generator

6.3.3.4 Low-side PWM with adaptive gate control, motor operating as generator

The control scheme during high-side PWM in generator mode (refer to **Figure 20**) is equivalent to low-side PWM in load mode with the complementary signal of the external PWM input.

The turn-on, turn-off delay times and the rise and fall times are applied and measured for the active MOSFET.

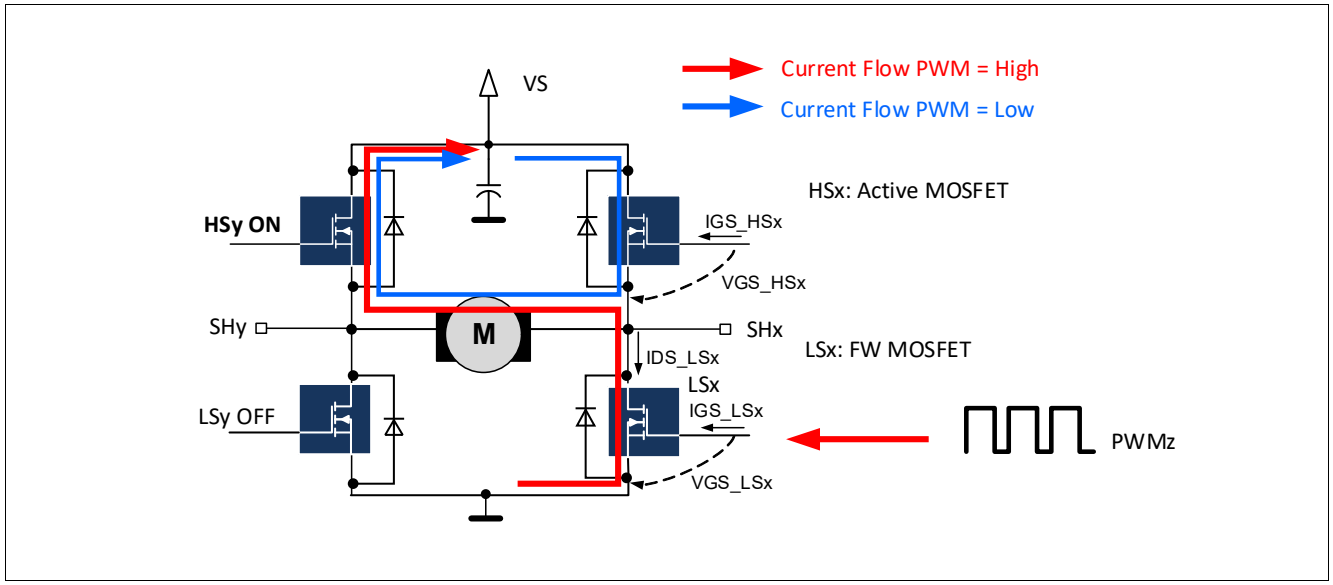


Figure 22 PWM input z is mapped to low-side x, the motor operating as generator

Floating gate drivers

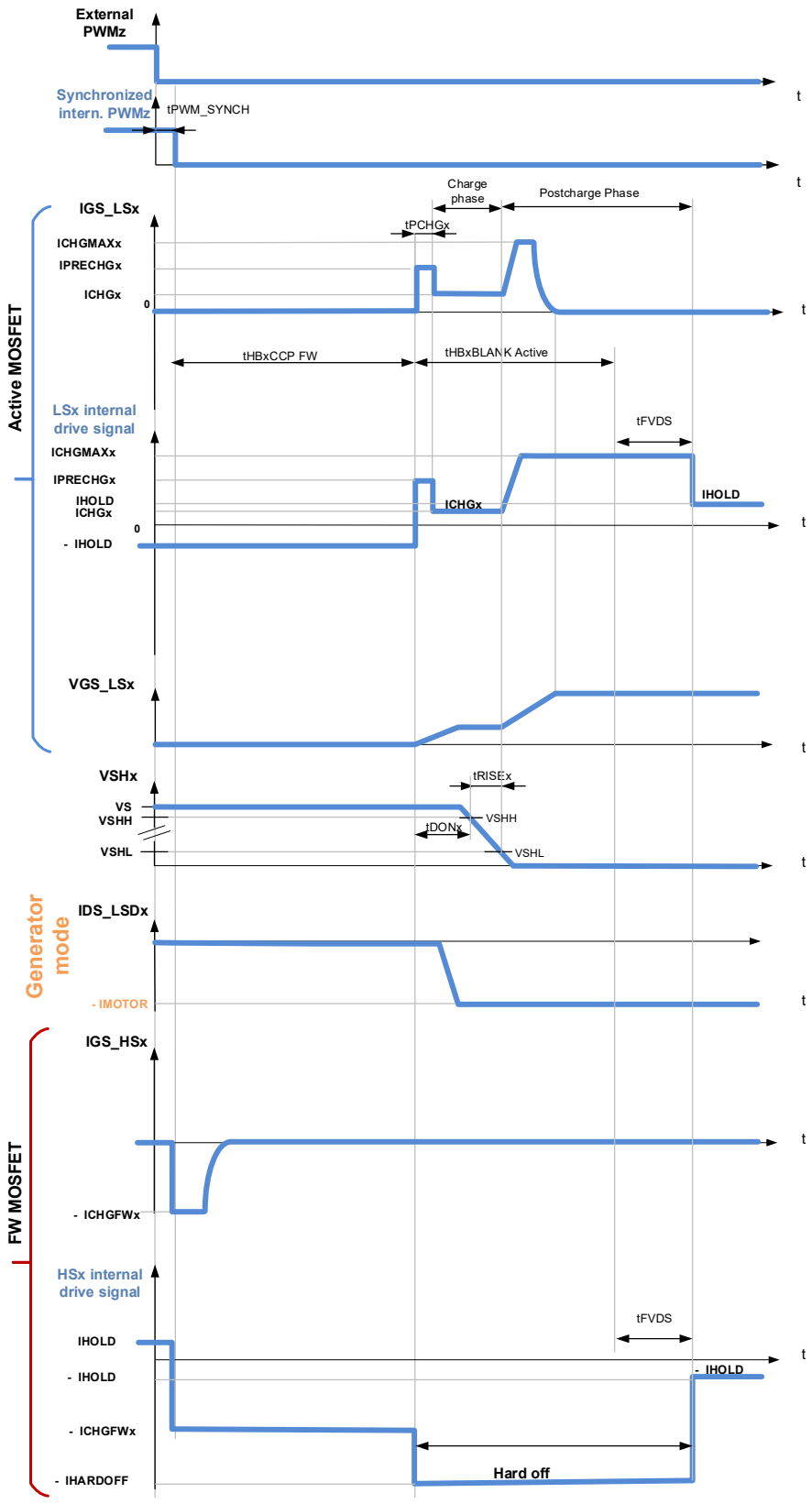


Figure 23 Adaptive turn-off with high-side PWM, AGC[1:0] = (1,0) or (1,1), motor operating as generator

6.3.3.5 Status bits for regulation of turn-on and turn-off delay times

The control bits TDREGx (**GENSTAT**) indicate if tDONx and tDOFFx of the PWM channel x using the adaptive gate control scheme (AGC[1:0] = 10_B or 11_B) is in regulation.

The PWM channel is considered in regulation if one of the following conditions are met:

- the effective turn-on and turn-off delays are equal to the configured delays for at least eight consecutive PWM cycles
- the error between the effective and configured delay changes its sign at least three times during the last 8 PWM cycles

6.3.3.6 Precharge and predischarge phases with EN_DEEP_AD = 1

This section is valid if **EN_DEEP_AD** = 1. Enabling this feature leads to a lower granularity of the resulting precharge and and predischarge currents.

This principle is illustrated with an example during the precharge phase on **Figure 24**. The same principle is applied to the predischarge phase.

If **EN_DEEP_AD** = 1:

- The precharge phase can be divided in two parts, during which different precharge current steps are applied
- The predischarge phase can be divided in two parts, during which different predischarge current steps are applied

The device exits the “deep adaptation mode” if t_{DON}, respectively t_{DOFF}, cannot be regulated and the resolution of the precharge time cannot be further divided. Then, one single current step is applied during the precharge time (**Figure 25**).

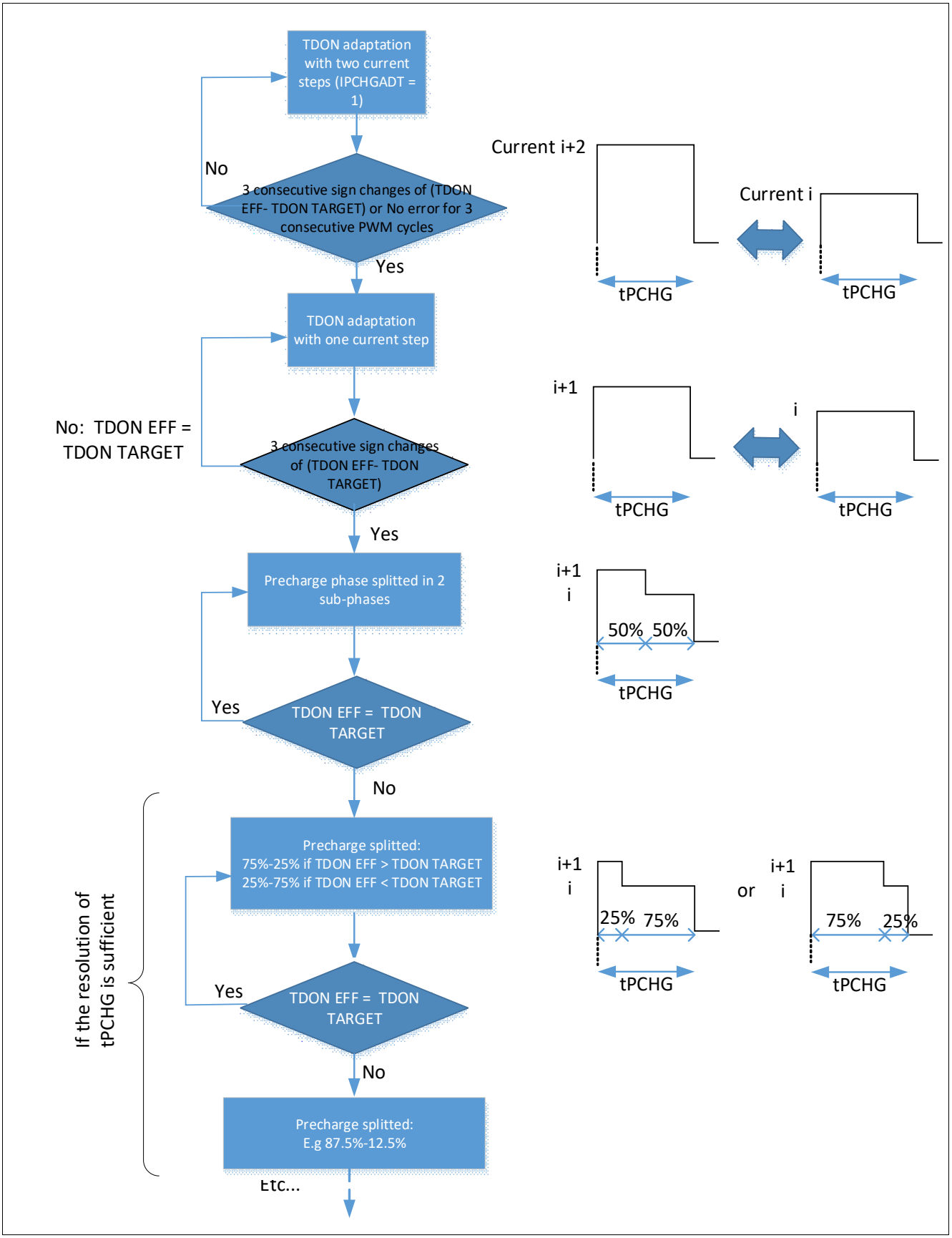


Figure 24 Example of precharge current modulation during the precharge phase, EN_DEEP_AD = 1

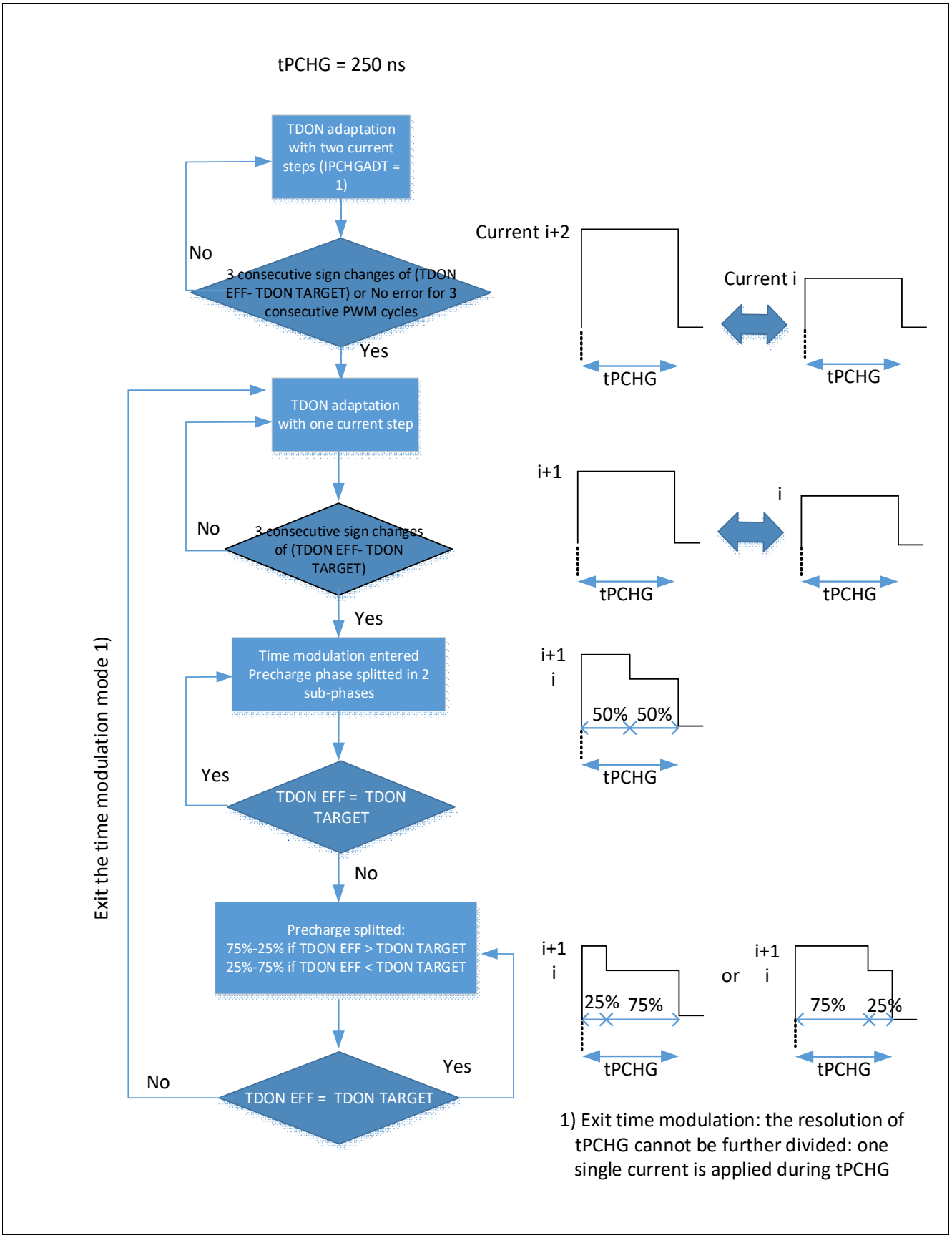


Figure 25 Criteria to exit the time modulation, EN_DEEP_AD = 1

6.3.4 PWM operation without adaptive gate control

The adaptive gate control is disabled if AGC[1:0] is set to (0,0) or (0,1). The effective turn-on and turn -off delays of the PWM MOSFETs are not regulated. Two modes can be selected.

The target turn-on and turn-off delay times of PWM MOSFETs (configured in **TDON_OFF1**, **TDON_OFF2**,**TDON_OFF3**) are no longer regulated. Nevertheless the status registers **EFF_TDON_OFF1**, **EFF_TDON_OFF2**, **EFF_TDON_OFF3** still report the effective turn-on and turn-off times of the PWM MOSFET.

6.3.4.1 PWM operation without adaptive gate control, AGC[1:0] = (0,0)

When AGC[1:0] = (0,0) (see **GENCTRL2**), the control of the gate drivers in PWM mode differs from the description of **Chapter 6.3.3**, **PWM operation with adaptive gate control**, only by the suppression of the pre-charge and pre-discharge phases.

6.3.4.2 PWM operation without adaptive gate control, AGC[1:0] = (0,1)

When AGC[1:0] = (0,1) (see **GENCTRL2**), the control of the gate drivers in PWM mode differs from the description of **Chapter 6.3.4.1**, **PWM operation without adaptive gate control, AGC[1:0] = (0,0)**, only by the addition of a pre-discharge phase. During tPDCHGz, the gate of the PWM MOSFET mapped to the PWM channel z is discharged with the current -IPDCHGINITz (Refer to **PWM_PDCHG_INIT**).

Refer to **Figure 26** for the turn-off of the PWM MOSFET with high-side PWM.

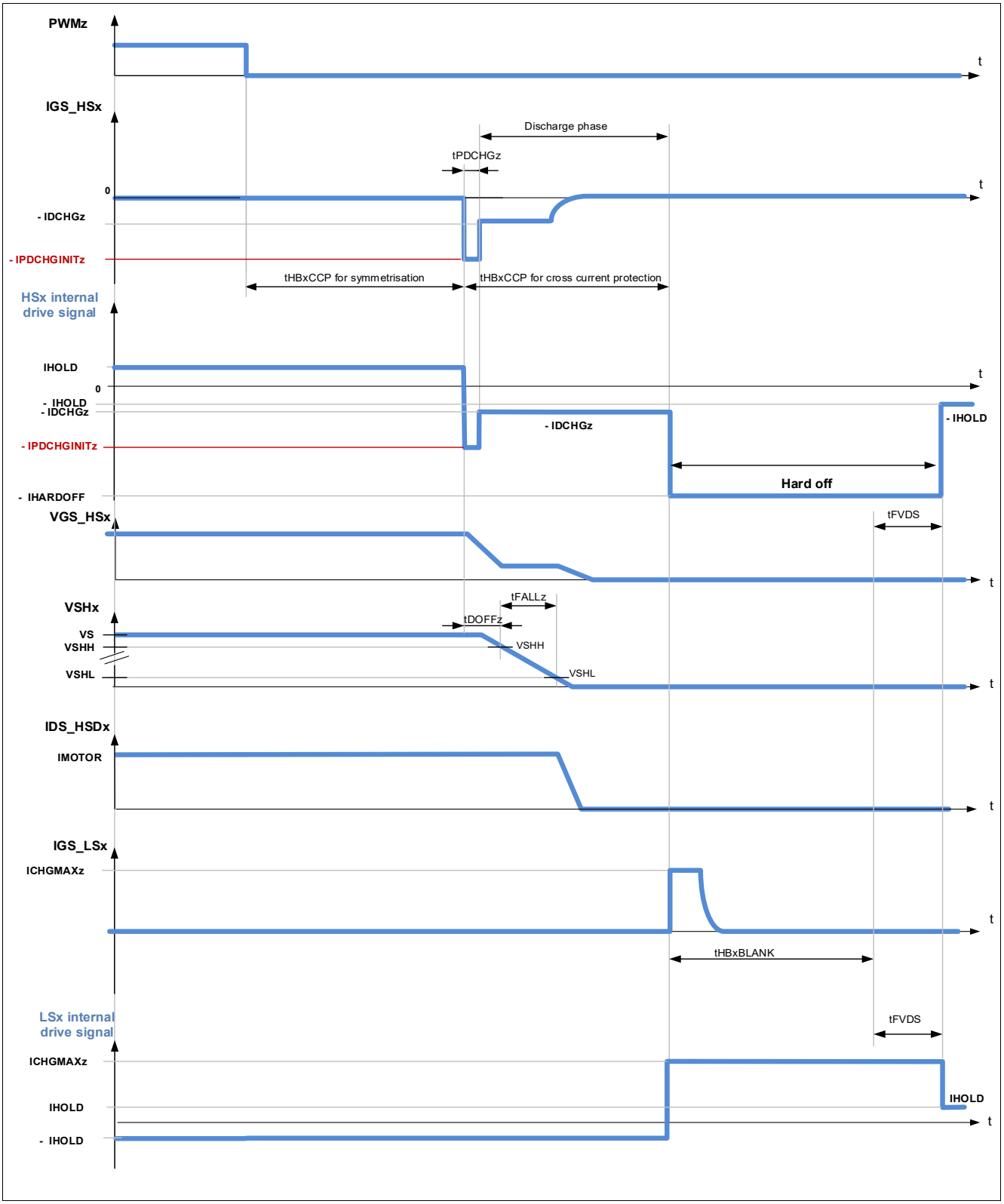


Figure 26 High-side PWM operation - turn-off without adaptive gate control, AGC[1:0] = (0,1)

6.3.5 PWM operation at high and low duty cycles

This section describes the internal PWM signal of the active and FW MOSFET when the motor operates as load or generator. In particular, at low and high duty cycles, the active free-wheeling is disabled.

*Note: It is recommended to clear **EN_GEN_CHECK** (**EN_GEN_CHECK** to 0) at very high or very low duty cycles: tON < tHBxCCP FW or tOFF < tHBxCCP active. Under these conditions, a generator mode cannot be correctly detected. The control scheme of the active MOSFET and of the freewheeling MOSFET can therefore be inverted.*

Note: The device cannot measure the switching times tDON, tDOFF, tRISE and tFALL at very high or very low duty cycles: tON < tHBxCCP FW or tOFF < tHBxCCP active.

General case, motor operating as load, tON > tHBxCCP FW and tOFF > tHBxCCP active

Figure 27 shows the internal control signals of the PWM MOSFETs and the freewheeling MOSFET while the motor operates as load :

- tON is longer than the FW cross-current protection time (tHBxCCP FW)
- tOFF is longer than the active cross-current protection time (tHBxCCP Active)

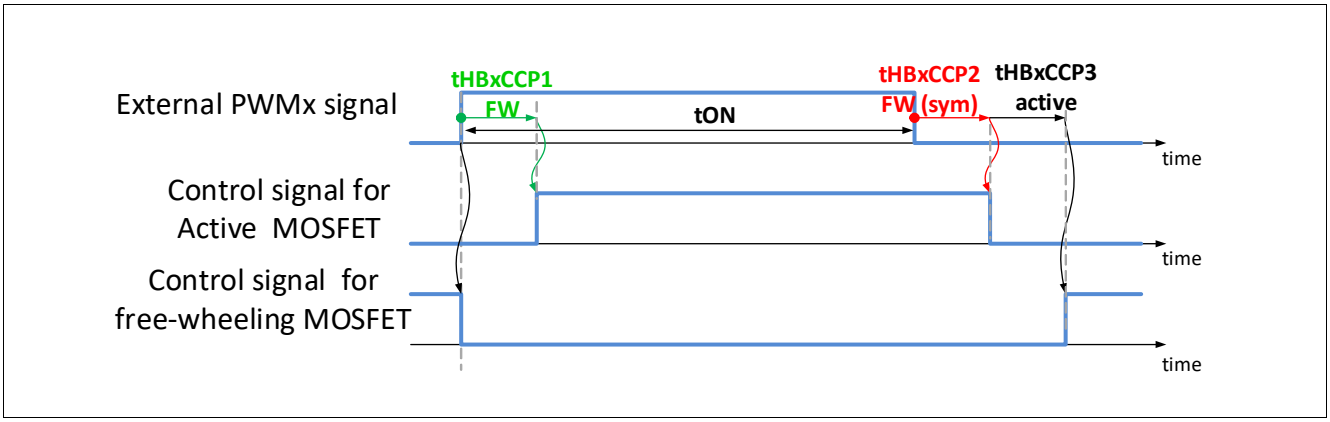


Figure 27 Internal signals for PWM operation - General case tON > tHBxCCP FW, tOFF > tHBxCCP active, motor operating as load

General case, motor operating as generator, tOFF > tHBxCCP FW and tON > tHBxCCP active

Figure 28 shows the internal control signals of the PWM MOSFETs and the freewheeling MOSFET while the motor operates as generator:

- tOFF is longer than the FW cross-current protection time (tHBxCCP FW)
- tON is longer than the active cross-current protection time (tHBxCCP Active)

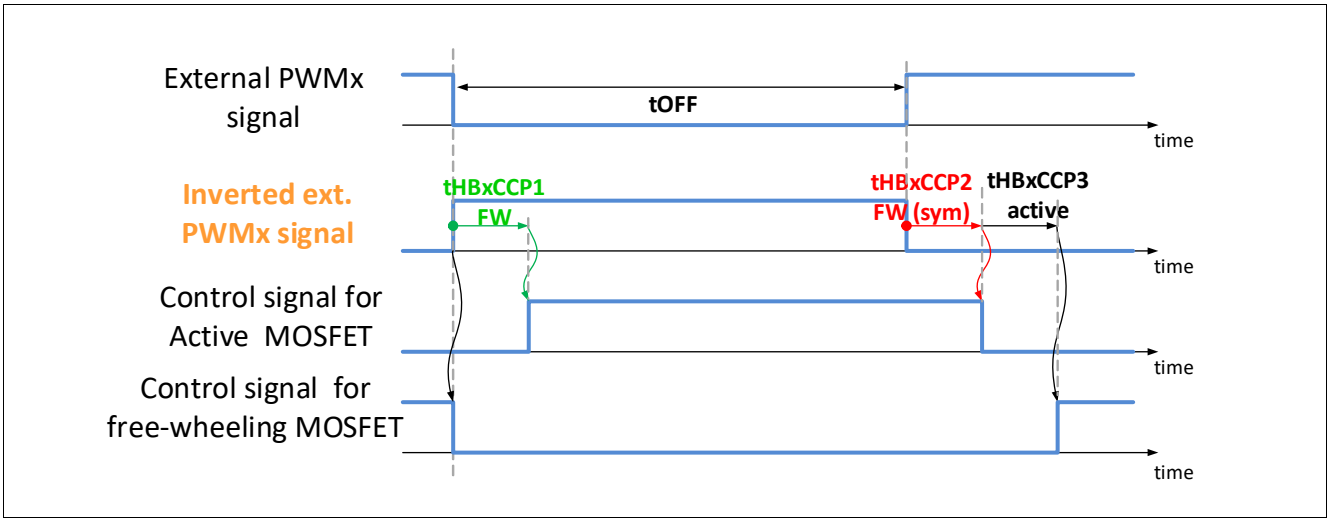


Figure 28 Internal signals for PWM operation - General case: tOFF > tHBxCCP FW, tON > tHBxCCP active, motor operating as generator

High duty cycle: tOFF < tHBxCCP active

No distinction between active MOSFET and FW MOSFET is possible, when the OFF-time of the external PWM signal is shorter than the configured active cross-current protection time. Therefore the PWM MOSFET (selected by HBxMODE[1:0]) is controlled as the active MOSFET. In other words, it is assumed that the motor operates as load. The control signal of the PWM MOSFET is shifted by one FW cross-current protection time compared to the external PWM signal. The MOSFET opposite to the PWM MOSFET stays OFF (passive FW). Refer to **Figure 29**.

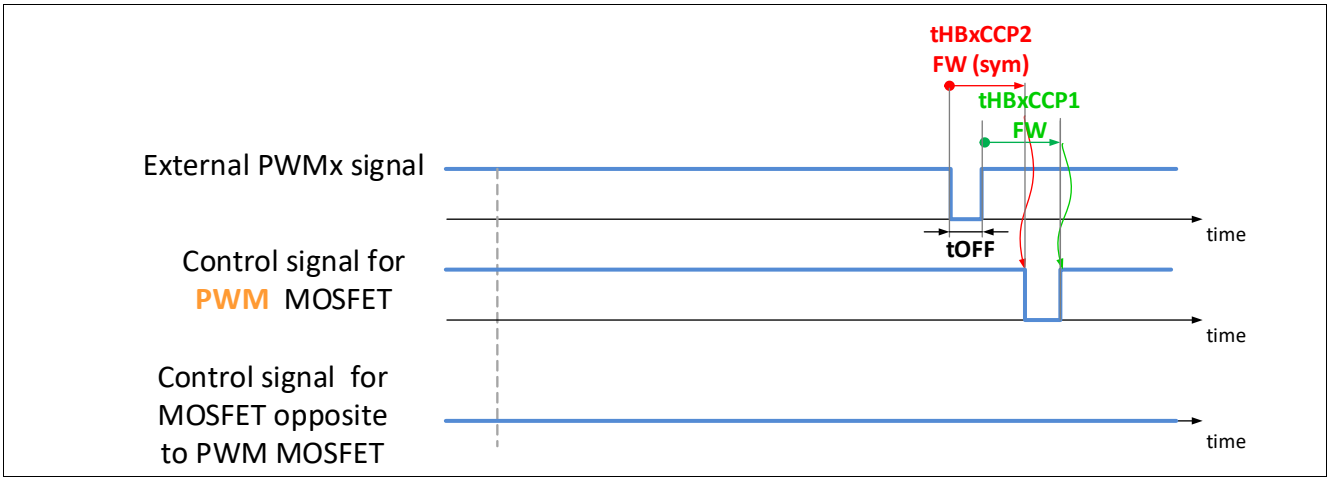


Figure 29 Internal signals for PWM operation at high duty cycle, tOFF < tHBxCCP active

Low duty cycle: tON < tHBxCCP FW

No distinction between active MOSFET and FW MOSFET is possible, when the ON-time of the external PWM signal is shorter than the configured FW cross-current protection time. Therefore the PWM MOSFET (selected by HBxMODE[1:0]) is controlled as the active MOSFET. In other words, it is assumed that the motor operates as load. The control signal of the PWM MOSFET is shifted by one cross-current protection time compared to the external PWM signal. Refer to **Figure 30**.

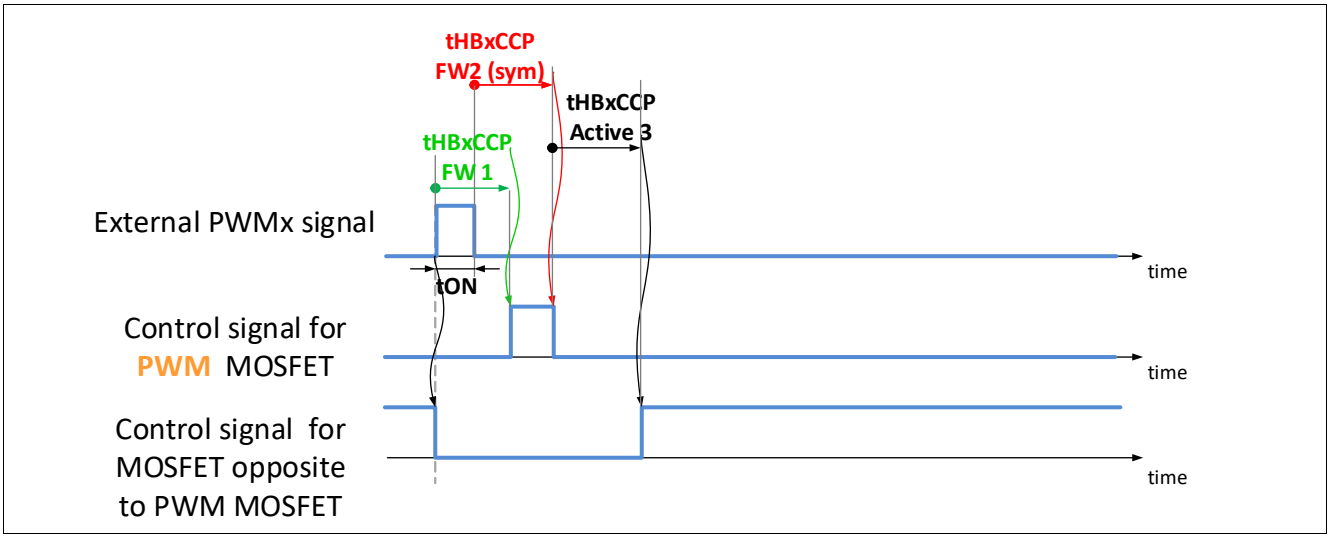


Figure 30 Internal signals for PWM operation at low duty cycle, tON < tHBxCCP FW

6.3.6 Gate driver current

Each gate driver is able to source and sink currents from 1.0 mA to 100 mA, with 32 steps according to **Figure 31** and **Figure 32**.

The charge and discharge currents of the active and the FW MOSFETs are configured separately by:

- The **REG_BANK** bit (**GENCTRL1**)
- The control registers **PWM_ICHG_ACT**, **PWM_IDCHG_ACT**, **PWM_ICHG_FW**

The charge current of the active MOSFETs are configured by **PWM_ICHG_ACT** (**REG_BANK** = 0)
The discharge current of the active MOSFETs are configured by **PWM_IDCHG_ACT** (**REG_BANK** = 0)
The charge and discharge current of the FW MOSFET are configured by **PWM_ICHG_FW** (**REG_BANK** = 1)

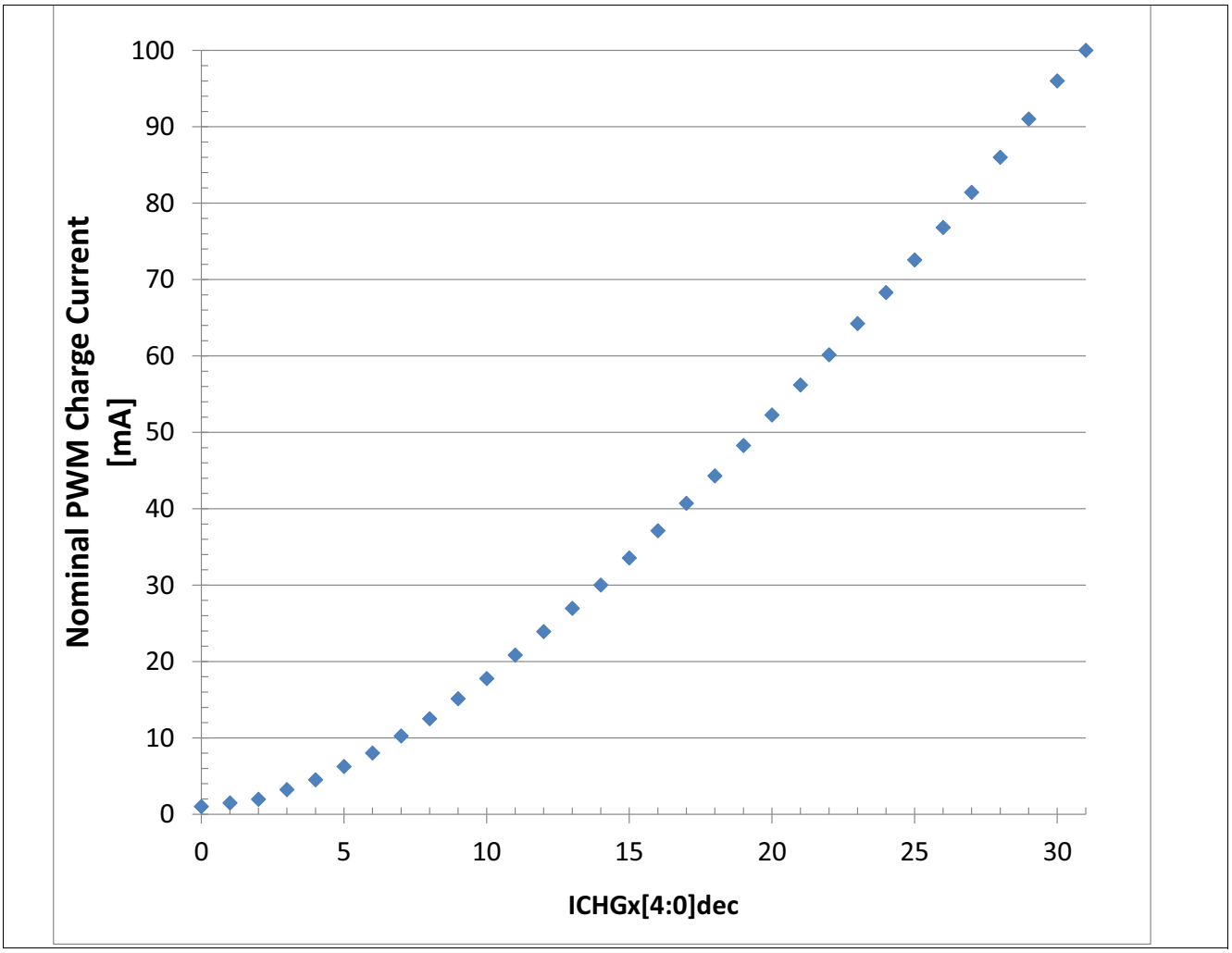


Figure 31 Configurable charge currents in PWM operation

Table 13 Charge currents in PWM operation

ICHGx[4:0], ICHGxFW[4:0], IPCHGINITx[4:0]	Nom. charge current [mA][1)]	Max. deviation to nominal values [%]
00000_B	1.0	+/- 60 %
00001_B	1.5	+/- 60 %
00010_B	2.0	+/- 60 %
00011_B	3.2	+/- 60 %
00100_B	4.5	+/- 60 %
00101_B	6.3	+/- 60 %
00110_B	8.0	+/- 38 %
00111_B	10.3	+/- 38 %
01000_B	12.5	+/- 38 %
01001_B	15.1	+/- 38 %
01010_B	17.8	+/- 38 %
01011_B	20.8	+/- 38 %
01100_B	23.9	+/- 38 %
01101_B	27.0	+/- 38 %
01110_B	30.0	+/- 28 %
01111_B	33.5	+/- 28 %
10000_B	37.1	+/- 28 %
10001_B	40.7	+/- 28 %
10010_B	44.3	+/- 28 %
10011_B	48.3	+/- 28 %
10100_B	52.3	+/- 28 %
10101_B	56.2	+/- 28 %
10110_B	60.1	+/- 28 %
10111_B	64.2	+/- 28 %
11000_B	68.3	+/- 28 %
11001_B	72.5	+/- 28 %
11010_B	76.8	+/- 28 %
11011_B	81.4	+/- 28 %
11100_B	86.0	+/- 28 %
11101_B	91.0	+/- 28 %
11110_B	96.0	+/- 25 %
11111_B	100	+/- 25 %

1) $V_S \geq 8V$ and $V_{GS} \leq V_{GS(ON)1}$ if ICHGx/ICHGxFW $\leq 14_D$, $V_S \geq 8V$ and $V_{GS} \leq V_{GS(ON)2}$ if ICHGx/ICHGxFW $\geq 15_D$

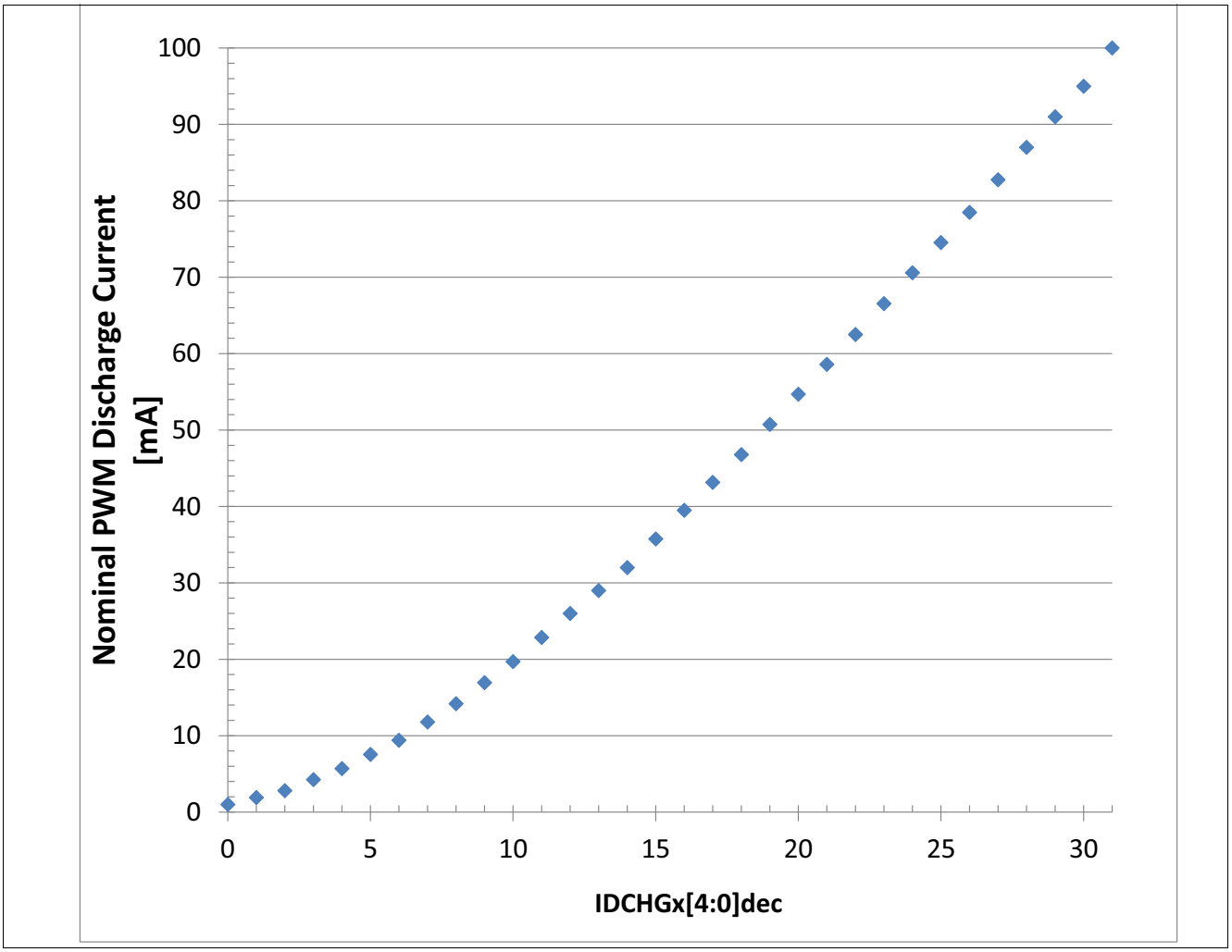


Figure 32 Configurable discharge currents in PWM operation

Table 14 Discharge currents in PWM operation

IDCHGx[4:0], IDCHGxFW[4:0], IPDCHGINITx[4:0]	Nom. discharge current [mA][1)]	Max. deviation to nominal values [%]
00000_B	1.0	+/- 60 %
00001_B	1.9	+/- 60 %
00010_B	2.8	+/- 60 %
00011_B	4.3	+/- 60 %
00100_B	5.7	+/- 60 %
00101_B	7.5	+/- 60 %
00110_B	9.4	+/- 38 %
00111_B	11.8	+/- 38 %
01000_B	14.2	+/- 38 %
01001_B	17.0	+/- 38 %
01010_B	19.7	+/- 38 %
01011_B	22.9	+/- 38 %
01100_B	26.0	+/- 38 %
01101_B	29.0	+/- 38 %
01110_B	32.0	+/- 28 %
01111_B	35.8	+/- 28 %
10000_B	39.5	+/- 28 %
10001_B	43.1	+/- 28 %
10010_B	46.8	+/- 28 %
10011_B	50.8	+/- 28 %
10100_B	54.7	+/- 28 %
10101_B	58.6	+/- 28 %
10110_B	62.5	+/- 28 %
10111_B	66.6	+/- 28 %
11000_B	70.6	+/- 28 %
11001_B	74.6	+/- 28 %
11010_B	78.5	+/- 28 %
11011_B	82.8	+/- 28 %
11100_B	87.0	+/- 28 %
11101_B	91.0	+/- 28 %
11110_B	95.0	+/- 25 %
11111_B	100	+/- 25 %

1) $V_{GS} \geq V_{GS(OFF)1}$ if IDCHGx $\leq 14_D$, $V_{GS} \geq V_{GS(OFF)2}$ if IDCHGxFW $\geq 15_D$

6.4 Passive discharge

Resistors (R_{GGND}) between the gate of GHx and GND, and between GLx and GND, ensure that the external MOSFETs are turned off, when EN = Low or when $V_{DD} < V_{DDPOffR}$.

During normal mode with **BD_PASS** bit reset (**GENCTRL2**) without failure causing the deactivation of the gate drivers, these pull-down resistors are switched off. The MOSFET are actively kept off with the discharge current IHOLD.

During normal mode with failure leading to the deactivation of the gate drivers (charge pump undervoltage, VS undervoltage and overvoltage, thermal shutdown) or in fail safe mode, R_{GGND} are activated, independently from the setting of **BD_PASS**.

Gate driver power down

The gate driver is deactivated in normal mode with **BD_PASS** set to 1 **and** all HBxMODE[1:0]=00 or 11. The current consumption of the VS input is reduced to $I_{S\_BD\_PASS}$ and R_{GGND} are activated.

6.5 Bridge driver in passive mode

The low-side MOSFETs LS1, LS2, LS3 and LS4 can be controlled when the bridge driver in the passive mode. All the other MOSFETs kept off by the passive discharge.

The bridge driver is in passive mode:

- If **BD_PASS** = 1 in normal mode and all HBxMODE[1:0]=00_B or 11_B.
- In sleep mode (EN = Low).
- If $V_{DD} < V_{DD\ POffR}$.

When the bridge driver is in passive mode, then the state of the low-side MOSFETs LS1-LS4 is configured by **PASS_MOD**.[1)]

- If PASS_MOD[1:0] = 00_B : LS1, LS2, LS3 and LS4 are off (passive discharge).
- If PASS_MOD[1:0] = 01_B : LS1, LS2, LS3 and LS4 are on (static brake).
- If PASS_MOD[1:0] = 10_B : LS1, LS2, LS3 and LS4 are turned on if $V_S > V_{SOV\ PASS\ OFF}$ (overvoltage brake). The PWM3 pin is pulled down by an internal open drain (R_{PWM3_OD}).
- If PASS_MOD[1:0] = 11_B : LS1, LS2, LS3 and LS4 are turned on if PWM1 = High and $V_S > V_{SOV\ PASS\ OFF}$ (overvoltage brake conditioned by PWM1). The PWM3 pin is pulled down by an internal open drain (R_{PWM3_OD}).

LS1, LS2, LS3 and LS4 MOSFETs with an input capacitor up to 10 nF are turned on within $t_{ON\_BD\_PASS}$.

The setting of LS1-LS4 according to **PASS_MOD** in sleep mode or if $V_{DD} < V_{DD\ POffR}$ is valid only if V_S stays above V_{SLEEP_SET}. If V_S drops below V_{SLEEP_SET}, then LS1-LS4 behave as if **PASS_MOD** = 10_B, the latter setting is kept even after a V_S recovery. Note that the quiescent current is changed accordingly.

1) If **BD_PASS** = 0, the setting by PASS_MOD[1:0] is effective only when EN= 0 or VDD < VDD POffR

6.6 Electrical characteristics gate driver

The electrical characteristics related to the gate driver are valid for $V_{CP} > V_S + 8.5$ V.

Table 15 Electrical characteristics: gate drivers

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C $V_{CP} > V_S + 8.5$ V, all voltages with respect to ground. Positive current flowing into pin except for I_{GLx} and I_{GHx} (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Comparators							
SHx High Threshold	V_{SHH}	V_S - 2.5	–	V_S - 2.0	V		P_6.5.1
SHx Low Threshold	V_{SHL}	2	–	2.5	V	Referred to GND	P_6.5.2
SHx comparator delay	t_{SHx}	–	5	30	ns	1)	P_6.5.26
MOSFET Driver Output							
High Level Output Voltage GHx vs. SHx and GLx vs. SL, CPSTGA= 0	V_{GH1}	10	–	12	V	V_S > 8 V C_{Load} = 10 nF I_{CP} = - 12 mA 2)	P_6.5.3
High Level Output Voltage GHx vs. SHx and GLx vs. SL, CPSTGA= 0	V_{GH3}	7	–	–	V	V_S > 6.0 V C_{Load} = 10 nF I_{CP} = - 6 mA 2)	P_6.5.5
High Level Output Voltage GHx vs. SHx and GLx vs. SL, CPSTGA= 1	V_{GH4}	10	–	12	V	1) V_S > 18 V, C_{Load} = 10 nF I_{CP} = - 12 mA 2)	P_6.5.6
Charge current	I_{CHG0}	0.4	1.0	1.6	mA	ICHG = 0_D C_{Load} = 10 nF $V_{GS} \le V_{GS(ON)1}$	P_6.5.30
Charge current	I_{CHG6}	5.0	8.0	11.0	mA	ICHG = 6_D C_{Load} = 10 nF $V_{GS} \le V_{GS(ON)1}$	P_6.5.31
Charge current	I_{CHG14}	21.6	30.0	38.4	mA	ICHG = 14_D C_{Load} = 10 nF $V_{GS} \le V_{GS(ON)1}$	P_6.5.33
Charge current	I_{CHG30}	72	96	120	mA	ICHG = 30_D C_{Load} = 10 nF $V_{GS} \le V_{GS(ON)2}$	P_6.5.35
Discharge current	I_{DCHG0}	-1.6	-1.0	-0.4	mA	IDCHG = 0_D C_{Load} = 10 nF $V_{GS} \ge V_{GS(OFF)1}$	P_6.5.36
Discharge current	I_{DCHG6}	-13.0	-9.4	-5.8	mA	IDCHG = 6_D C_{Load} = 10 nF $V_{GS} \ge V_{GS(OFF)1}$	P_6.5.37
Discharge current	I_{DCHG14}	-41.0	-32.0	-23.0	mA	IDCHG = 14_D C_{Load} = 10 nF $V_{GS} \ge V_{GS(OFF)1}$	P_6.5.39

Table 15 Electrical characteristics: gate drivers (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C V_{CP} > V_S + 8.5 V, all voltages with respect to ground. Positive current flowing into pin except for I_{GLx} and I_{GHx} (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Discharge current	I_{DCHG30}	-119	-95	-71	mA	IDCHG = 30_D C_{Load} = 10 nF $V_{GS} \geq V_{GS(OFF)2}$	P_6.5.41
Passive discharge resistance between GHx/GLx and GND	R_{GGND}	10	20	30	kΩ	1)	P_6.5.11
Resistor between SHx and GND	R_{SHGND}	10	20	30	kΩ	1)	P_6.5.12
Low RDSON mode	R_{ONCCP}	–	22	40	Ω	V_S = 13.5 V $V_{CP} = V_S$ + 14 V $I_{CHG} = I_{DCHG}$ = 31 (max)	P_6.5.13
Gate Drivers Dynamic Parameters							
External MOSFET gate-to-source voltage - ON	$V_{GS(ON)1}$	9	–	–	V	1) $V_S \geq$ 8V ICHGx ≤ 14_D	P_6.5.50
External MOSFET gate-to-source voltage - ON	$V_{GS(ON)2}$	7	–	–	V	1) $V_S \geq$ 8V ICHGx ≥ 15_D	P_6.5.51
External MOSFET gate-to-source voltage - OFF	$V_{GS(OFF)1}$	–	–	2	V	1) IDCHGx ≤ 14_D	P_6.5.53
External MOSFET gate-to-source voltage - OFF	$V_{GS(OFF)2}$	–	–	5	V	1) IDCHGx ≥ 15_D	P_6.5.53
PWM synchronization delay	t_{PWM_SYNCH}	50	–	150	ns	1)	P_6.5.46
Pre-charge time	t_{PCHG00}	100	125	150	ns	1) TPCHG = 00_B	P_6.5.18
Pre-charge time	t_{PCHG01}	200	250	300	ns	1) TPCHG = 01_B	P_6.5.19
Pre-charge time	t_{PCHG10}	400	500	600	ns	1) TPCHG = 10_B	P_6.5.20
Pre-charge time	t_{PCHG11}	800	1000	1200	ns	1) TPCHG = 11_B	P_6.5.21
Pre-discharge time	$t_{DPCHG00}$	100	125	150	ns	1) TDPCHG = 00_B	P_6.5.22
Pre-discharge time	$t_{DPCHG01}$	200	250	300	ns	1) TDPCHG = 01_B	P_6.5.23
Pre-discharge time	$t_{DPCHG01}$	400	500	600	ns	1) TDPCHG = 10_B	P_6.5.24
Pre-discharge time	$t_{DPCHG01}$	800	1000	1200	ns	1) TDPCHG = 11_B	P_6.5.25

1) Not subject to production test, specified by design.

2) ICHGx[4:0] = 11111_B (100 mA typ.)

7 Protections and diagnostics

7.1 Reverse polarity protection

The output of the charge pump (CP pin) can be used to supply an external n-channel MOSFET, building an active reverse polarity protection. Refer to **Figure 50**.

7.2 Safe switch (optional)

The output of the charge pump (CP pin) can be used to supply an optional external n-channel MOSFET, operating as safe switch. The safe switch can be actively turned off for example by the microcontroller or a safety logic, in order to disconnect the MOSFET supply, independently from the TLE92104-232. Refer to **Figure 50**.

7.3 Drain-source voltage monitoring with bridge driver in active mode

When EN =High and **BD_PASS** = 0 (bridge driver in active mode), voltage comparators monitor the activated MOSFETs to protect the high-side MOSFETs and low-side MOSFETs against a short circuit respectively to ground and to the battery during ON-state.

If a Drain-Source overvoltage is detected, the corresponding half-bridge is latched off.

If HBxD = 0, x =1..4 (**VDS1**): The half-bridge x is latched off if the voltage difference between DH and VSHx exceeds the threshold voltage configured by **VDS1** (see **Table 16**).

If HBxD = 1, x =1..4 (see **VDS1**): The half-bridge x is latched off if the voltage difference between CSIN1 and VSHx exceeds the threshold voltage configured by **VDS1** (see **Table 16**).

Short circuits of low-side MOSFETs to VS are detected by monitoring the voltage difference between VSHx and SL (see **Table 16**).

Table 16 Drain-Source overvoltage threshold, EN = High, BD_PASS= 0

HBxVDSTH[1)][2:0]	Drain-Source overvoltage threshold for HSx and LSx[1)] (typical)
000_B	150 mV
001_B	200 mV (default)
010_B	250 mV
011_B	300 mV
100_B	400 mV
101_B	500 mV
110_B	600 mV
111_B	2 V

1) x = 1 … 4.

Attention: ***HBxVDSTH[2:0] = 111_B (2 V threshold) is dedicated for the diagnostic in off-state. It is highly recommended to select another drain-source overvoltage threshold once the routine of the diagnostic in off-state has been performed to avoid additional current consumption from VS and from the charge pump.***

The device reports a Drain-Source overvoltage error if both conditions are met:

- After expiration of the blank time.
- If the Drain-Source voltage monitoring exceeds the configured threshold for a duration longer than the configured filter time (refer to **Table 17** and **GENCTRL2** TFVDS bits).

Table 17 Drain-Source overvoltage filter time

TFVDS[1:0]	Drain-Source overvoltage filter time (typical)
00_B	0.5 µs (default)
01_B	1 µs
10_B	2 µs
11_B	3 µs

If a short circuit is detected by the Drain-Source voltage monitoring:

- The impacted half-bridge is latched off.
  - The discharge current is according to the settings of **ST_ICHG**, as if the MOSFET was previously statically activated.
- The corresponding bit in the status register **DSOV** is set.
- The VDSE in Global Status Register **Global status byte** is set.

If a Drain-Source overvoltage is detected for one of the MOSFETs, then the status register **DSOV** must be cleared in order to re-enable the faulty half-bridge.

7.4 Drain-source voltage monitoring with bridge driver in passive mode

LS1 to LS4 can be activated when the bridge driver is in passive mode (refer to **Chapter 6.5**).

A drain-source overvoltage monitoring of LS1, LS2, LS3 and LS4 MOSFETs is enabled if **PASS_VDS** is set.

The drain-source monitoring (VSHx - VSL, x = 1 to 4) is ignored for $t_{BLK\_BD\_PASS}$ (blank time) after beginning of the activation of LS1, LS2, LS3 and LS4 MOSFETs.

The drain-source monitoring filter time is $t_{DSMON\_FILT\_BD\_PASS}$ and the VDS threshold is $V_{VDSMON\_BD\_PASS}$ (370 mV typ).

If a drain-source overvoltage is detected, then:

- The LS1, LS2, LS3 and LS4 MOSFETs are turned off.
- **PASS_VDSOV** and the corresponding status bit in **DSOV** are set.

LS1-4 can be reactivated by clearing **DSOV**. Clearing **DSOV** also clears **PASS_VDSOV**.

7.5 Cross-current protection and drain-source overvoltage blank time

All gate drivers feature a cross-current protection time and a Drain-Source overvoltage blank times.

The cross-current protection avoids the simultaneous activation of the high-side and the low-side MOSFETs of the same half-bridge.

During the blank time, the drain-source overvoltage detection is disabled, to avoid a wrong fault detection during the activation phase of a MOSFET.

Notes

1. *The setting of the cross-current protection and of the blank times may be changed by the microcontroller only if all PWMx_EN bits are reset, x = 1 … 3.*
2. *Changing the Drain-Source overvoltage of a half-bridge x (HBx) in on-state (HBxMODE[1:0]=(0,1) or (1,0)) may result in a wrong VDS overvoltage detection on HBx. Therefore it is highly recommended to change this threshold when HBxMODE[1:0]=(0,0) or (1,1).*

7.5.1 Cross-current protection

Four pairs of cross-current protection and blank times ((tCCPx, tBLANKx), x = 1…4) can be mapped to each half-bridge with the control register **CCP_BLK1**.

The cross-current protection time of the active MOSFET of the FW MOSFETs are set independently.

- The cross-current protection times of the active MOSFETs are configured by the control bits TCCPx_ACT (**CCP_BLK2_ACT**, **PWM_ICHGMAX_CCP_BLK3_ACT**) and **CCP_BLK1**
- The cross-current protection times of the free-wheeling MOSFETs are configured by the control bits TCCPx_FW (**CCP_BLK2_FW**, **PWM_ICHGMAX_CCP_BLK3_FW**) and **CCP_BLK1**

Table 18 Cross-current protection time

TCCPx_ACT[2:0], TCCPx_FW[2:0],x = 1…4	Cross-current protection time tCCPx_ACT/tCCPx_FW, x = 1…4 (typical)
000_B	375 ns
001_B	625 ns
010_B	1 µs
011_B	1.5 µs
100_B	2 µs (default)
101_B	3 µs
110_B	4 µs
111_B	16 µs[1)]

1) When applying a cross-current protection time of 16 µs to a half-bridge, the max. drive current used for this half-bridge must be set below 30 mA to avoid an overheating of the gate driver.

7.5.2 Drain-source overvoltage blank time in bridge driver active mode

A configurable blank time (refer to **Table 19**) for the Drain-Source monitoring is applied at the turn-on of the MOSFETs. During the blank time, a Drain-Source overvoltage error is masked.

The blank time of the active MOSFET of the FW MOSFETs are set independently:

- The blank times of the active MOSFETs are configured by the control bits TBLANKx_ACT (**CCP_BLK2_ACT**, **PWM_ICHGMAX_CCP_BLK3_ACT**) and **CCP_BLK1**
- The blank times of the free-wheeling MOSFETs are configured by the control bits TBLANKx_FW (**CCP_BLK2_FW**, **PWM_ICHGMAX_CCP_BLK3_FW**) and **CCP_BLK1**

Half-bridges in PWM mode

If the detection of the generator mode is disabled (**EN_GEN_CHECK** = 0):

- The blank time of the PWM MOSFET starts at the expiration of the cross-current protection time of the FW MOSFET (tHBxCCP FW). Refer to **Figure 33**.

- The blank time of the FW MOSFET starts after expiration of the cross-current protection time at turn-off of the PWM MOSFET (tHBxCCP Active). Refer to **Figure 33**.

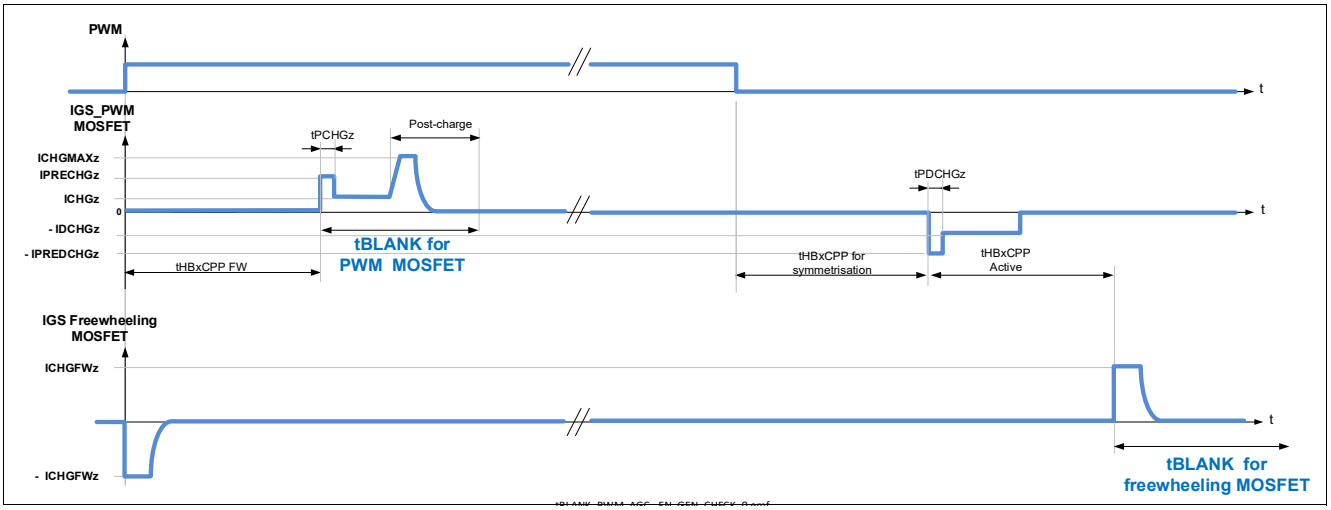


Figure 33 Blank time for half-bridges in PWM operation, detection of generator mode disabled (EN_GEN_CHECK = 0)

If the detection of the generator mode is enabled (**EN_GEN_CHECK** = 1):

- The blank time of the Active MOSFET starts at the expiration of the cross-current protection time of the FW MOSFET (tHBxCCP FW). Refer to **Figure 34** and **Figure 35**.
- The blank time of the FW MOSFET starts after expiration of the cross-current protection time at turn-off of the Active MOSFET (tHBxCCP Active). Refer to **Figure 34** and **Figure 35**.

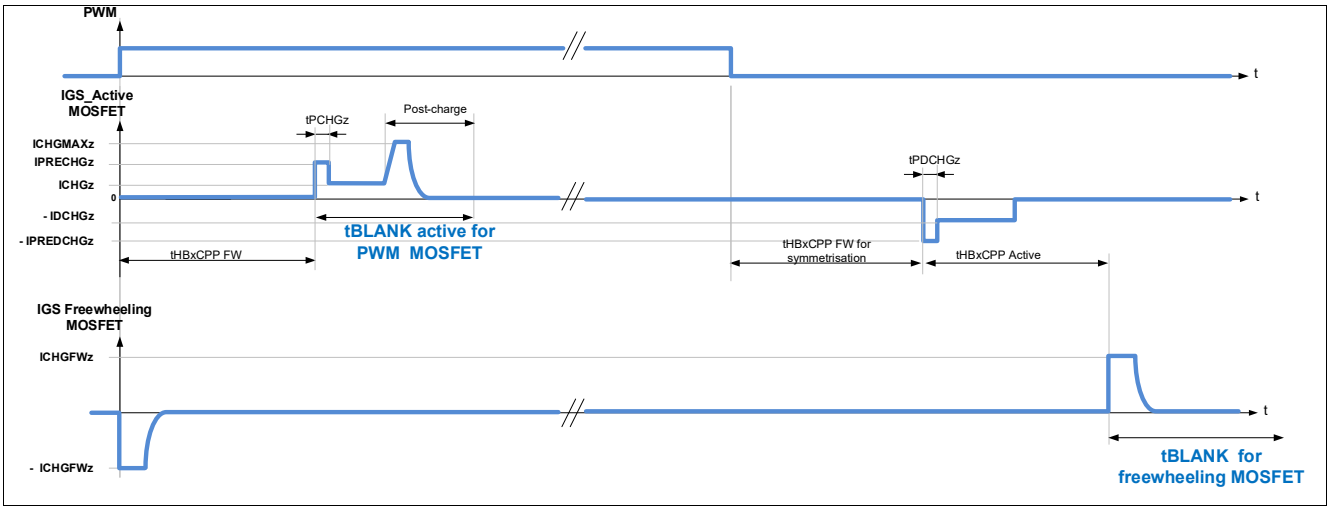


Figure 34 Blank time for half-bridges in PWM operation, detection of generator mode enabled (EN_GEN_CHECK = 1), motor operating as load

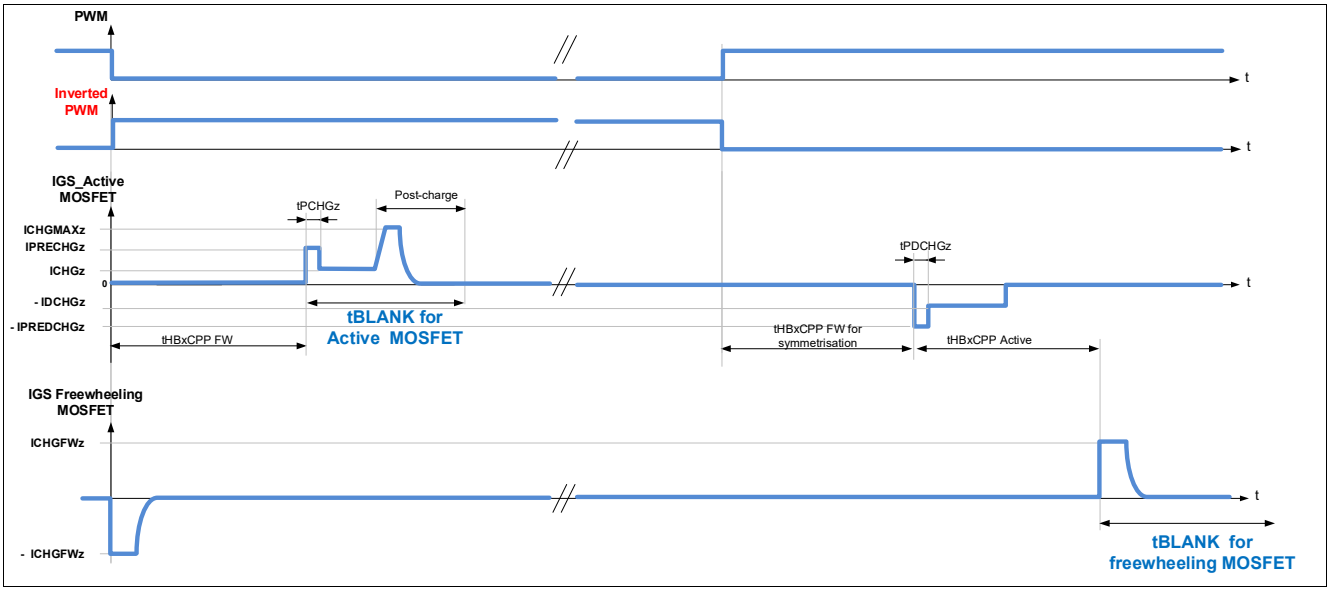


Figure 35 Blank time for half-bridges in PWM operation, detection of generator mode enabled (EN_GEN_CHECK = 1), motor operating as generator

For statically activated half-bridges, the blank time starts:

- Case 1: At expiration of the active cross-current protection (**Figure 7**), if the opposite MOSFET was previously activated.
- Case 2: Right after the decoding of the SPI command to turn on a MOSFET, if the half-bridge was in high impedance (**Figure 8**).

The blank times can be configured with the control registers **CCP_BLK2_ACT** and **PWM_ICHGMAX_CCP_BLK3_ACT** for the active MOSFETs and **CCP_BLK2_FW** and **PWM_ICHGMAX_CCP_BLK3_FW** for the freewheeling MOSFETs.

Table 19 Drain-source overvoltage blank time

TBLANKx[2:0], x = 1…4	Drain-Source overvoltage blank time tBLANKx, x = 1…4 (typical)
000_B	625 ns
001_B	1 µs
010_B	1.25 µs
011_B	1.5 µs
100_B	2 µs (default)
101_B	3 µs
110_B	4 µs
111_B	16 µs[1)]

1) When applying a blank time of 16 µs to a half-bridge, the max. drive current used for this half-bridge must be set below 30 mA , to avoid an overheating of the gate driver.

Note: The blank time is implemented at every new activation of a MOSFET, including a recovery from VS undervoltage, VS overvoltage.

7.5.3 Mapping of cross-current protection and blank times

One of the pairs of cross-current protection and blank times are mapped to each half-bridge according to **Table 20**, by configuring the control register **CCP_BLK1**.

Table 20 Mapping of tCCP and tBLANK to the half-bridges

HBxCCPBLK[1:0],x =1..4	tCCP and tBLANK applied to HBx
00_B	(tCCP1,tBLANK1) are mapped to HBx[1)]
01_B	(tCCP2,tBLANK2) are mapped to HBx
10_B	(tCCP3,tBLANK3) are mapped to HBx
11_B	(tCCP4,tBLANK4) are mapped to HBx

1) Example: (tHBxCCP, tHBxBLANK) = (tCCP1, tBLANK1), x = 1 … 4.

7.6 OFF-state diagnostic

In order to support the off-state diagnostic, the gate driver of each MOSFET provides pull-up (450 µA typ.) and a pull-down currents (1250 µA typ.) at the SHx pins when the driver driver is active (**BD_PASS** = 0). Under these conditions, the pull-up current sources are active.

Attention: The off-state diagnostic is possible only when the bridge driver is active (BD_PASS=0) and the corresponding half-bridge is off (HBxMODE = 00b or 11b).

The pull-down current of each gate driver are activated by the control bits HBxIDIAG (**HBIDIAG** register).

During the off-state diagnostic routine performed by the microcontroller, the drain-source overvoltage threshold of the relevant half-bridges must be set to 2 V nominal. Refer to **Table 16**. Once the routine is finished, it is highly recommended to decrease the drain-source overvoltage threshold to a lower value, avoiding additional current consumption from the VS input.

The following failures can be detected:

- MOSFET short circuit to GND.
- MOSFET short circuit the battery.
- Open load (disconnected motor).

The status of the output voltages VOUTx, with x = 1 … 4, can be read back with status bit HBxVOUT (register **HBVOUT_PWMERR**) when the corresponding half-bridge is in off-state (HBxMODE[1:0] = 00 or 11).

Note: HBxVOUT = 0 if the half-bridge x is not in off-state (HBxMODE[1:0] = (0,1) or (1,0)).

Refer to **Application information**, **Chapter 10** for off-state diagnostic when the shunt resistor is in the motor phase.

7.7 Temperature monitoring

Temperature sensors are integrated in the device. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds.

Temperature warning

If the temperature sensor reaches T_{jW}, then **TW** is set (see **GENSTAT**). This bit is latched and reset by clearing **GENSTAT** if the thermal warning condition has disappeared. The outputs stages however remain activated. Refer to **Figure 36**.

Temperature shutdown

If the temperature sensor reaches T_{jSD} **all gate drivers are latched off, the charge pump is deactivated** ; the SUPE bit (Supply Error bit, see **Global status byte**), **TSD** (Thermal Shutdown bit) and **CPUV** (Charge Pump Undervoltage) are set (see **GENSTAT**). All outputs remain deactivated until the temperature shutdown condition has disappeared and **GENSTAT** is cleared. See **Figure 36**.

The discharge current is according to the settings of **ST_ICHG**, as if the MOSFET was previously statically activated.

To resume normal functionality of the gate drivers (in the event the overtemperature condition disappears, or to verify if the failure still exists) the microcontroller shall clear **GENSTAT**.

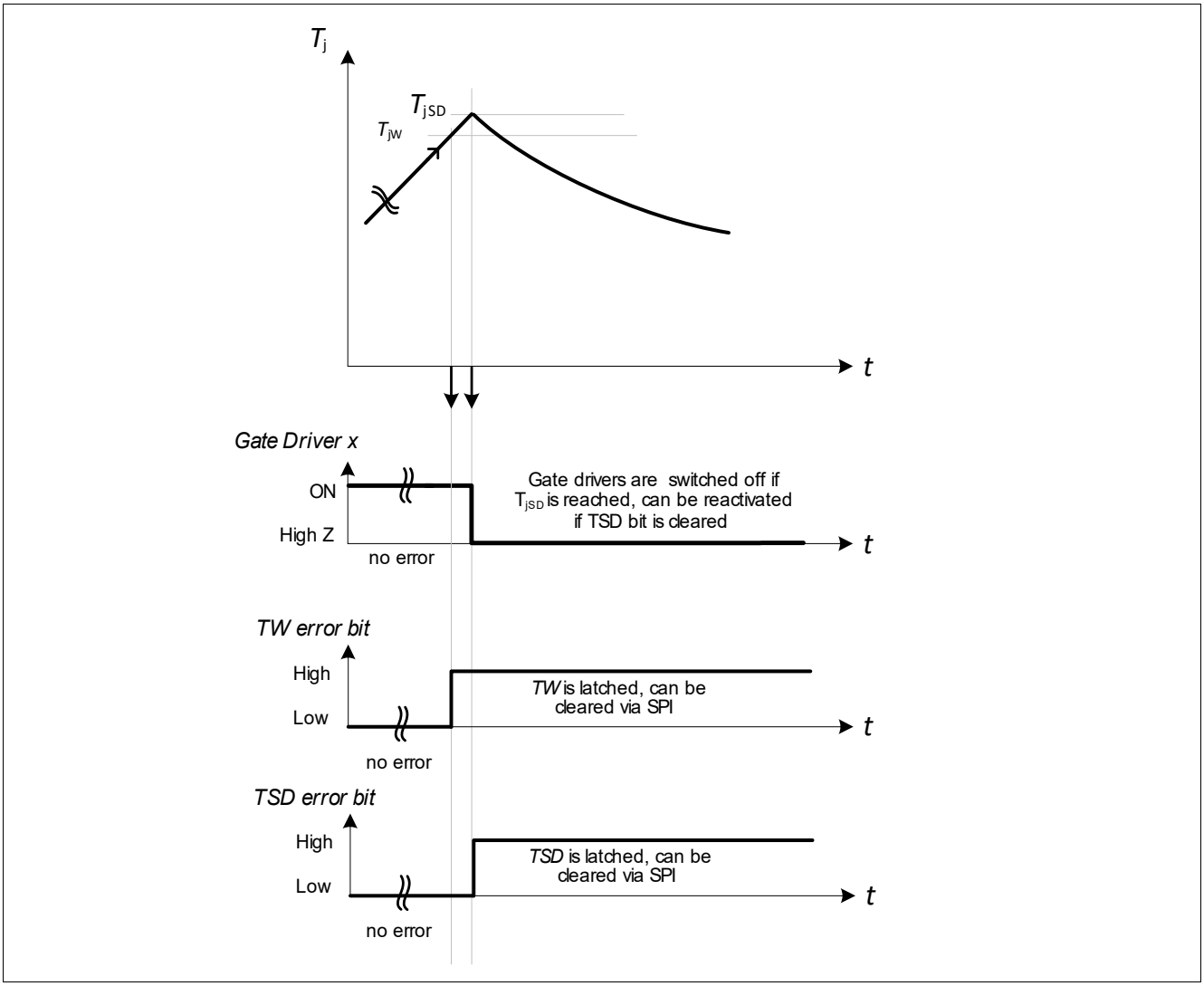


Figure 36 Overtemperature behavior

7.8 V_S overvoltage and undervoltage shutdown

The power supply rails V_S and V_{DD} are monitored for supply fluctuations. The V_S supply is monitored for under- and over-voltage conditions whereas the V_{DD} supply is monitored for under-voltage conditions.

7.8.1 V_S undervoltage

If V_S drops below $V_{SUV\ OFF}$, then all external MOSFETs are latched off, however, the logic information remains intact and uncorrupted provided that $V_{DD} > V_{DD\ POR}$.

SUPE (Supply Error bit, see **Global status byte**), **VSUV** and **CPUV** bits (see **GENSTAT**), are set and latched.

The **VSUV** bit is reset by clearing **GENSTAT** to re-enable the MOSFETs.

The **VSUV** bit is reset if the following conditions are fulfilled:

- $V_S > V_{SUV\ ON}$ (See **Figure 37**).
- The TLE92104-232 receives a clear command to **GENSTAT**.

7.8.2 V_S overvoltage with bridge driver in active mode

If V_S rises above the switch-off voltage ($V_{SOV\ OFF1}$ if VSOVTH= 0, $V_{SOV\ OFF2}$ if VSOVTH= 1) all external MOSFETs are latched off, and the charge pump is deactivated. SUPE bit (see **Global status byte**) , **VSOV** bit (V_S over-voltage bit, see **GENSTAT**), and CPUV bit are set and latched. If V_S decreases below $V_{SOV\ ON}$,then the charge pump is reactivated automatically. The **VSOV** bit must be reset to re-enable the MOSFETs.

The **VSOV** bit is reset if the following conditions are fulfilled:

- $V_S < V_{SOV\ ON}$ (See **Figure 37**).
- The TLE92104-232 receives a clear command to **GENSTAT**.

The discharge current is according to the settings of **ST_ICHG**, as if the MOSFET was previously statically activated.

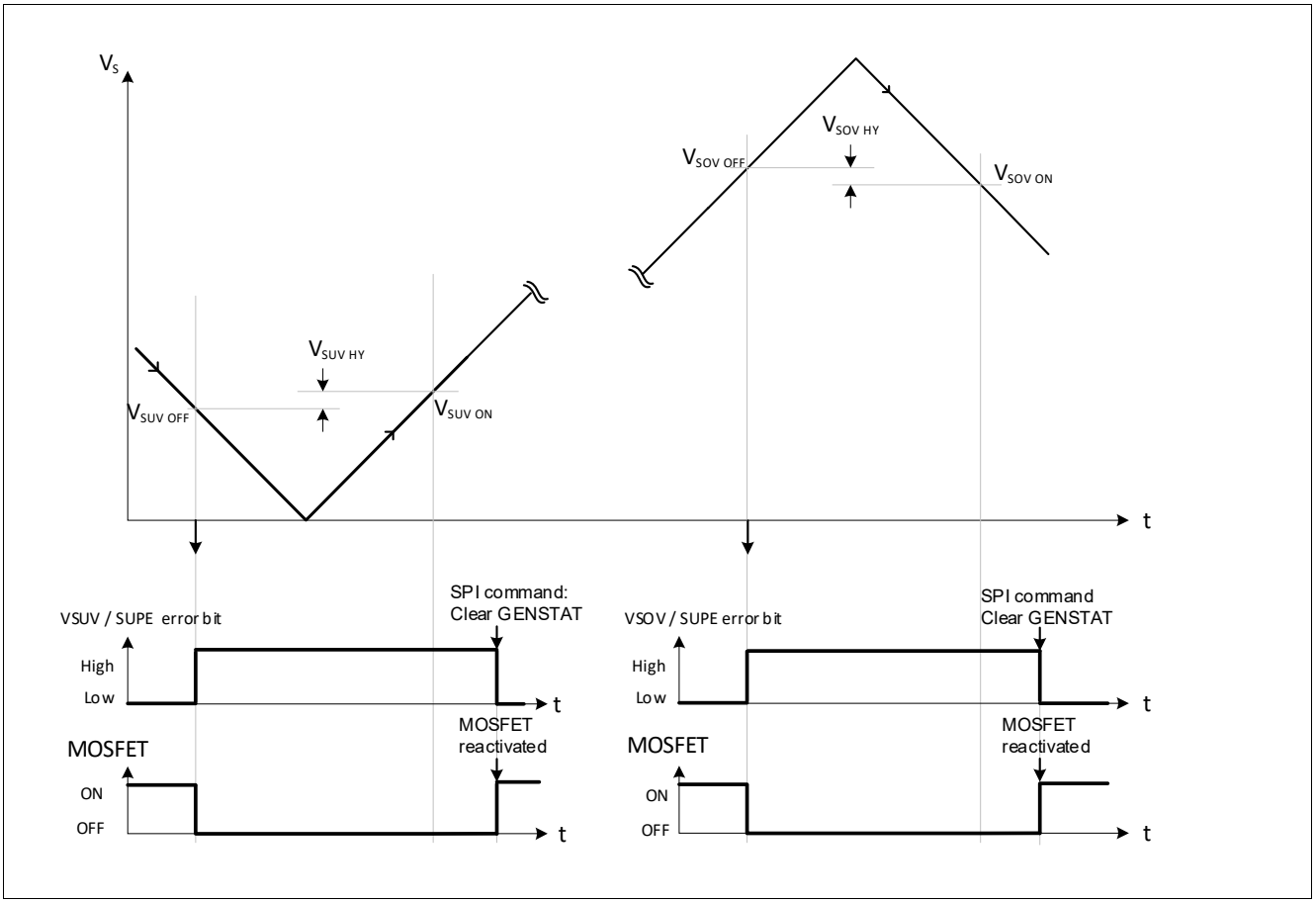


Figure 37 Output behavior during Over- and Undervoltage V_S condition

7.8.3 V_S overvoltage with bridge driver in passive mode

When the bridge driver is in passive mode (refer to **Chapter 6.5**):

- If PASS_MOD[1:0] = 10_B : LS1, LS2, LS3 and LS4 are turned on if VS > **$V_{SOV\ PASS\ OFF}$** (overvoltage brake). The PWM3 pin is pulled down by an internal open drain (**R_{PWM3_OD}**).
- If PASS_MOD[1:0] = 11_B : LS1, LS2, LS3 and LS4 are turned on if VS > **$V_{SOV\ PASS\ OFF}$** and PWM1 = High (overvoltage brake conditioned upon PWM1). The PWM3 pin is pulled down by an internal open drain (**R_{PWM3_OD}**).

If VS exceeds $V_{SOV\ PASS\ OFF}$, then all low-side MOSFETs are turned on within $t_{ON\_BD\_PASS}$.

7.8.4 V_{DD} undervoltage

If the V_{DD} logic supply decreases below the undervoltage threshold, $V_{DD\ POffR}$, the SPI interface shall no longer be functional. The digital block will be reset and the gate drivers are switched off.The undervoltage reset is released once V_{DD} voltage is above the undervoltage threshold, $V_{DD\ POR}$.

7.8.5 Charge pump undervoltage

The voltage of the charge pump output (VCP) is monitored in order to ensure a correct control of the external MOSFETs.

If VCP falls below the configured charge pump undervoltage threshold:

- The external MOSFETs are actively discharged for the duration tHBxCCP with the current ICHGSTx, then the gate drivers are turned off.
- **CPUV** (**GENSTAT**), SUPE bits (**Global status byte**) and the Global Error Flag (**Chapter 8.2**) are set and latched.

The **CPUV** and SUPE bits are reset and the normal operation is resumed if **GENSTAT** is cleared, and VCP > VCPUV.[1)]

Notes

1. *A charge pump undervoltage event is reported after a power-on reset, when the charge time of the capacitor connected to VCP exceeds* t_{CPUV}.
2. *The charge pump is is deactivated after a VS undervoltage, a VS overvoltage and a thermal shutdown, causing a charge pump undervoltage condition. Consequently **CPUV** and SUPE bits are set together with **VSOV**, **VSUV** or **TSD** bits (see **GENSTAT**).*

7.9 Switching parameters of MOSFETs in PWM mode

The effective switching parameters of the active MOSFETs (**EN_GEN_CHECK** =1) or of the PWM MOSFET (**EN_GEN_CHECK** =0) can be read out with dedicated status registers:

- The turn-on and turn off delays, noted tDON and tDOFF, are reported by the status register **EFF_TDON_OFF1**, **EFF_TDON_OFF2**, **EFF_TDON_OFF3**.
- The rise and fall times, noted tRISE and tFALL, are reported by the status register **TRISE_FALL1**, **TRISE_FALL2**, **TRISE_FALL3**.

Refer to **Chapter 6.3** for the definition of tDON, tDOFF, tRISE and tFALL.

If tHBxBLANK active has elapsed in motor mode, before the measurement of the effective tDON , the device reports an effective tDON corresponding to tHBxBLANK active.

If tHBxCCP active has elapsed while **EN_GEN_CHECK** =0[2)], before the measurement of the effective tDOFF, the device reports an effective tDOFF corresponding to tHBxCCP active.

7.10 Timeout watchdog

An integrated timeout watchdog supervises the integrity of the communication with the microcontroller.

The watchdog period is programmable by the **WDPER** bit (refer to **GENCTRL1**).

After a Power-On Reset, the watchdog timer starts and the microcontroller must invert the logic value of the **WDTRIG** bit of the control register **GENCTRL1**. The default value of **WDTRIG** is 0. A correct trigger of the watchdog immediately resets the watchdog counter and starts the next cycle.

A watchdog failure is reported by the device if:

- The watchdog trigger bit is not served within the watchdog period (watchdog timeout event). See **Figure 38**[3)].
- The microcontroller writes the **WDTRIG** bit with the same value. In other words, if the **WDTRIG** value is 0 and the microcontroller re-writes **WDTRIG** to 0, or the **WDTRIG** is 1, and the microcontroller re-writes **WDTRIG** to 1, then a watchdog error is reported.

1) Recovering from VS under/overoltage and thermal shutdown, CPUV bit can be cleared only after 64 µs
2) If **EN_GEN_CHECK**= 1 and tDOFF cannot be measured until the expiration of tHBxCCP, then the device considers that the motor operate as as generator
3) WDMON[1:0] (**GENSTAT**) is not reset after a WD timeout when the WD period is configured to 50 ms

If a watchdog failure is detected, then the FS bit (see Global Status Byte) is set and latched, and the control registers are frozen to their default values. Consequently all external MOSFETs are actively turned off.

In order to resume normal operation, the microcontroller must: 1. clear **GENSTAT**. 2. Set **WDTRIG** to 1 within the watchdog period, 3. Set **WDTRIG** to 0 within the watchdog period[1)].

The watchdog period is configurable by SPI to T_{WDPER1} or T_{WDPER2} (refer to **WDPER**).

Monitoring the watchdog timer

The status bits **WDMON**[1:0] report the relative position of the watchdog timer to the watchdog period. Refer to **Table 21** and **Figure 38**. This allows the detection of a potential latent failure associated to the watchdog timer: the microcontroller can indeed verify that the watchdog timer is running.

Table 21 Monitoring of the watchdog timer

WDMON[1:0]	Position of the watchdog timer
00_B	watchdog timer is between [0%, 25%[of the watchdog period
01_B	watchdog timer is between [25%, 50%[of the watchdog period
10_B	watchdog timer is between [50%, 75%[of the watchdog period
11_B	watchdog timer is between [75%, 100%[of the watchdog period

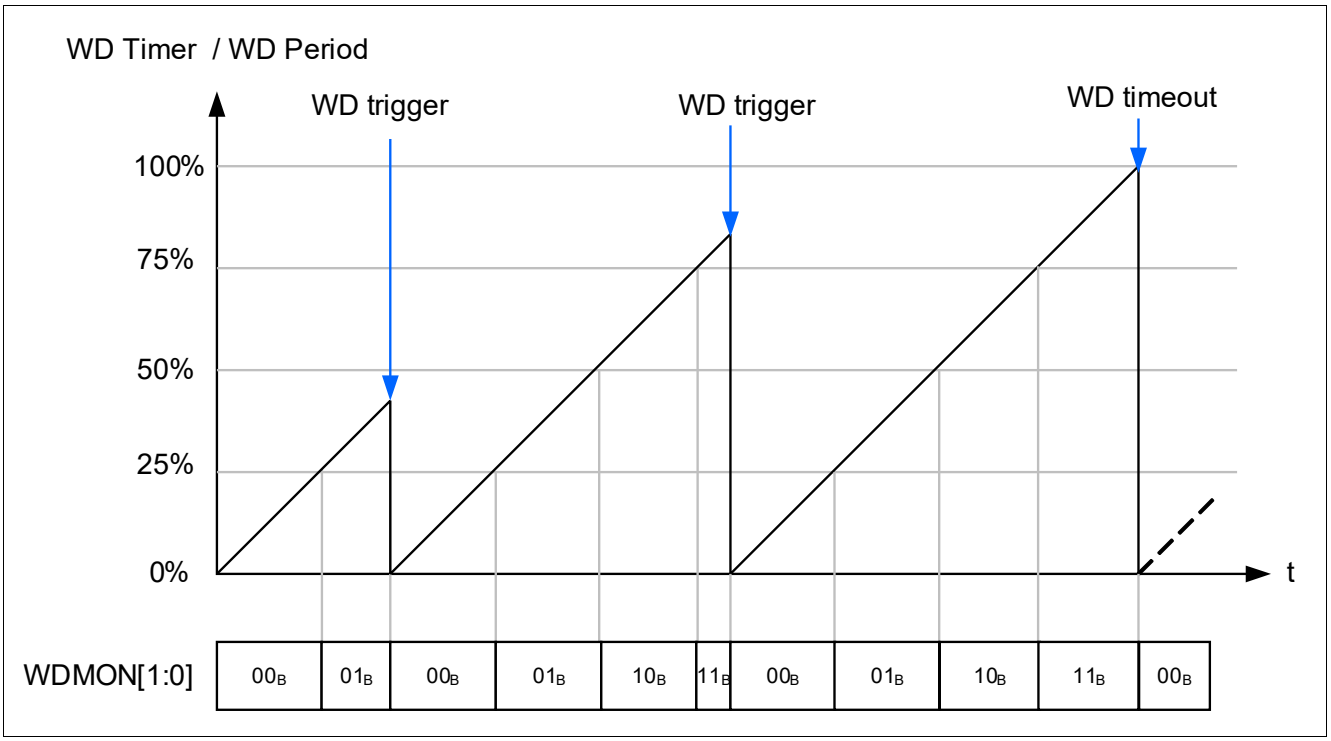


Figure 38 Example of watchdog monitoring and watchdog timeout

1) The exit sequence must be strictly followed to leave fail safe mode. If a SPI frame not belonging to the sequence is added (incl. a read command), then the device stays in fail safe mode and the microcontroller must restart the complete sequence to enter normal mode.

Disabling the watchdog

The watchdog is enabled by default.

It is disabled only if the following SPI sequence is sent:

- First frame: Set **UNLOCK** bit to '1' (**GENCTRL1**). Note: UNLOCK is automatically reset to '0' at the end of the following frame.
- Following frame: Set **WDDIS** bit to '1' (**GENCTRL2**).

The watchdog is directly re-enabled by setting WDDIS to '0'.

7.11 Current sense amplifier

Two current sense amplifiers allow to monitor the motor currents. The differential input stage measures the voltage drop across an external shunt resistor.

The input common mode range allows current sensing in high-side, in low-side configuration or in the motor phase.

7.11.1 Unidirectional and bidirectional operation

The current sense amplifiers (CSA) can work either as unidirectional or bi-directional CSA. See **CSD1** and **CSD2**.

Unidirectional operation CSDx = 0

In unidirectional operation, the CSAx, x = 1 or 2, is optimized to measure the current flowing through the external shunt resistor when VCSIPx ≥ VCSINx.
VCSOx = $V_{REF\ Unidir}$ + (VCSIPx - VCSINx + $\mathbf{V_{OS}}$) x G_{DIFF}, provided that VCSOx is in the linear range[1) 2)].

Bidirectional operation CSDx = 1

In bidirectional operation, the CSAx, x = 1 or 2, measures the current flowing through the external shunt resistor in both directions: VCSIPx ≥ VCSINx or VCSIPx ≤ VCSINx.
The output CSOx works at half-scale range: VCSOx = $V_{REF\ Bidir}$+ (VCSIPx - VCSINx + $\mathbf{V_{OS}}$) x G_{DIFF} provided that VCSOx is in the linear range [2)].

When the current sense amplifiers are deactivated (VS undervoltage, VS overvoltage, CP undervoltage or Overtemperature, or CSAx_OFF = 1), CSOx is pulled Low (between GND to 150 mV)

7.11.2 Gain configuration

The gain of the current sense amplifier is configurable by the configuration bits CSAGx bits. Refer to **Table 22** and **GENCTRL1**.

Table 22 Configuration of the current sense amplifier gain

CSAGx[1:0]	Typical current sense amplifier gain G_{DIFF}
00_B	10 V/V
01_B	20 V/V

1) Valid if 0.5 V ≤ VCSOx ≤ VDD - 0.5 V.
2) VCSOx is clamped between VDD and GND.

Table 22 Configuration of the current sense amplifier gain

CSAGx[1:0]	Typical current sense amplifier gain G_{DIFF}
10_B	40 V/V
11_B	80 V/V

7.11.3 High-side and low-side setting

The CSA can be used either in high-side configuration or in low-side configuration within the specified common mode range.

The control bits CSA1L and CSA2L (**HBIDIAG**) optimize the VDD current consumption by informing the device about the common mode voltage of the CSA inputs:

- CSAxL must be set to 0 if the shunt is in low-side configuration (i.e. connected to GND or to an output with an activated low-side).
- CSAxL must be set to 1 if the shunt is in high-side configuration (i.e.connected to VS or to an output with an activated high-side).

Notes

1. *A proper information from the CSA output is not ensured if the external shunt resistor is in high-side configuration while its CSAxL bit is set to 0.*
2. *The external shunt resistor may be in low-side configuration while its CSAxL bit is set to 1. The current consumption from VDD is however higher than if CSAxL is set to 0.*

7.11.4 Overcurrent detection

A comparator at CSOx detects overcurrent conditions. The overcurrent threshold is configurable with the OCTHx bits. Refer to **Table 23** for unidirectional operation and **Table 24** for bidirectional operation.

Table 23 Overcurrent detection thresholds in unidirectional operation (CSDx = 0)

OCTHx[1:0]	Typical Overcurrent Detection Threshold
00_B	$V_{CSOx} > V_{DD/2}$
01_B	$V_{CSOx} > V_{DD/2} + V_{DD}/10$
10_B	$V_{CSOx} > V_{DD/2} + 2 \times V_{DD}/10$
11_B	$V_{CSOx} > V_{DD/2} + 3 \times V_{DD}/10$

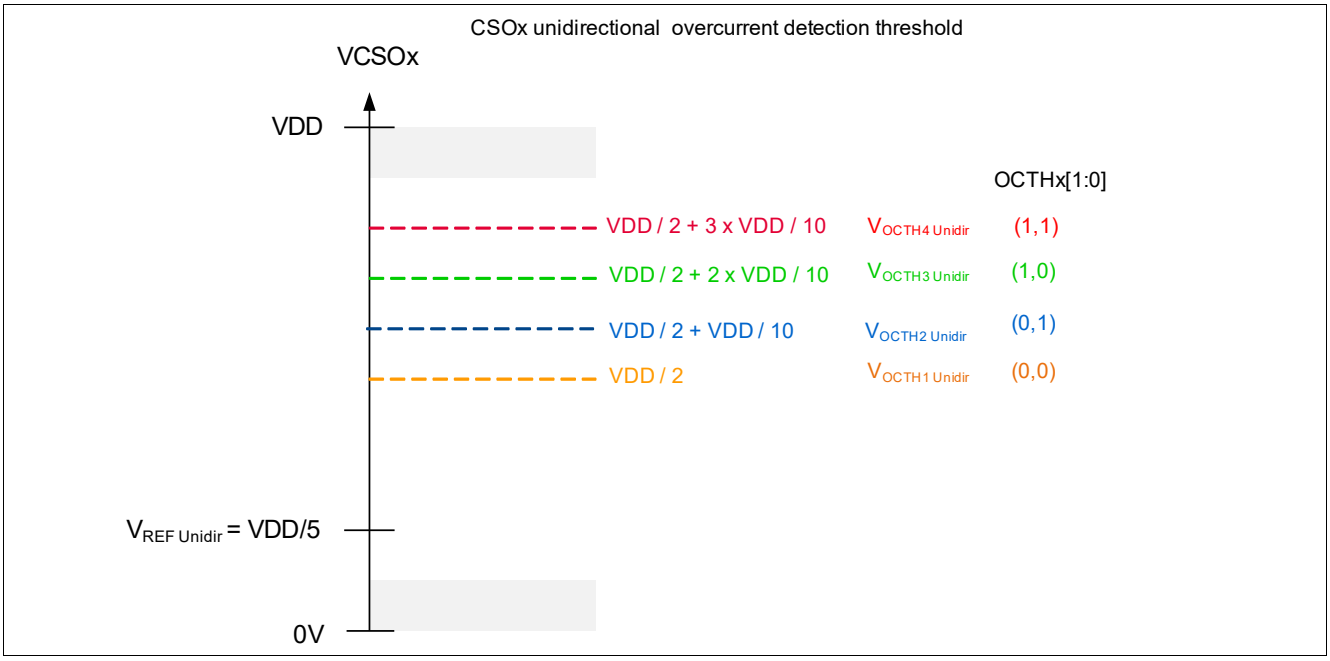


Figure 39 Overcurrent detection thresholds in unidirectional operation (CSDx = 0)

Table 24 Overcurrent detection thresholds in bidirectional operation (CSDx = 1)

OCTHx[1:0]	Typical Overcurrent Detection Threshold
00_B	$V_{CSOx} > V_{DD}/2 + 2 \times V_{DD}/20$ or $V_{CSOx} < V_{DD}/2 - 2 \times V_{DD}/20$
01_B	$V_{CSOx} > V_{DD}/2 + 4 \times V_{DD}/20$ or $V_{CSOx} < V_{DD}/2 - 4 \times V_{DD}/20$
10_B	$V_{CSOx} > V_{DD}/2 + 5 \times V_{DD}/20$ or $V_{CSOx} < V_{DD}/2 - 5 \times V_{DD}/20$
11_B	$V_{CSOx} > V_{DD}/2 + 6 \times V_{DD}/20$ or $V_{CSOx} < V_{DD}/2 - 6 \times V_{DD}/20$

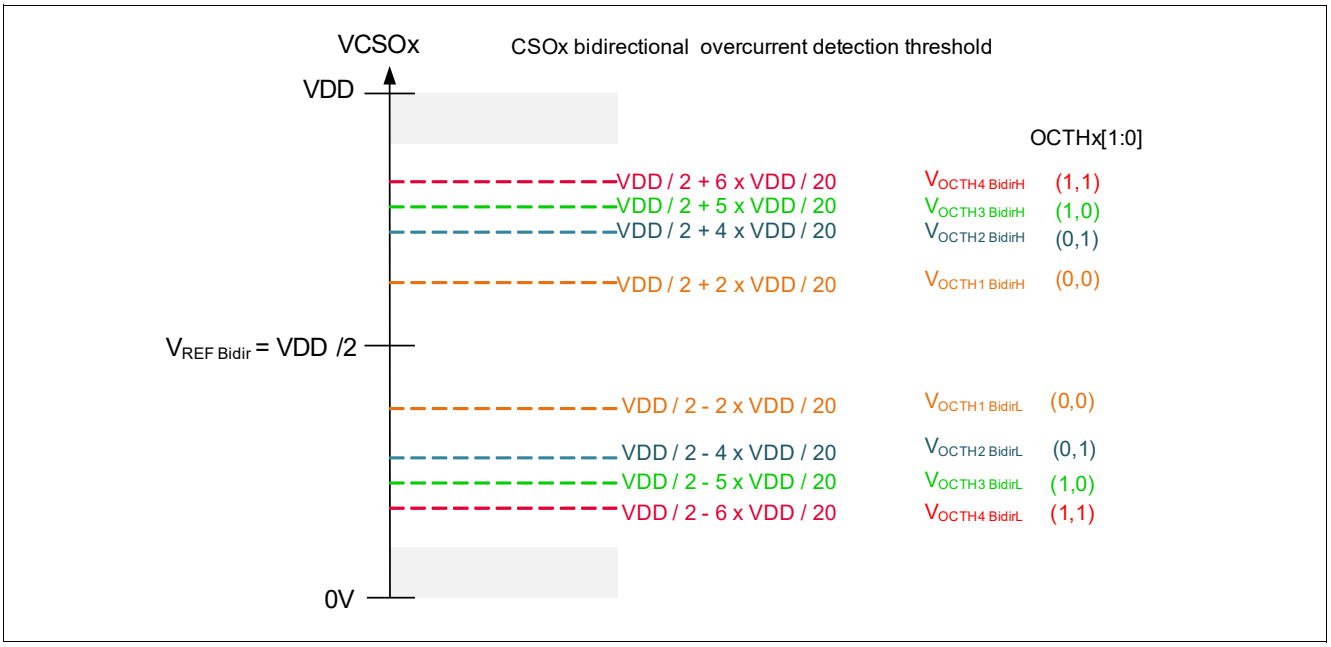


Figure 40 Overcurrent detection thresholds in bidirectional operation (CSDx = 1)

It is possible to program the device behavior when an overcurrent condition is detected:

- OCEN bit = 0 (see **GENCTRL1**): the device only reports the overcurrent event (OC, OC1 or OC2 in **GENSTAT** and Global Error Flag are set), without any change of the gate driver states
  - If the overcurrent condition is not present for more than t_{FOC}, then the overcurrent status bits are automatically cleared by the device.
- OCEN bit = 1 (see **GENCTRL1**): the device reports the overcurrent event (OC, OC1 or OC2 in **GENSTAT** and Global Error Flag are set) and turns off all MOSFETs with their static discharge current.
  - The MOSFETs can be reactivated by clearing **GENSTAT** or by resetting the OCEN bit.
  - The overcurrent status bits are reset only if the overcurrent condition is no longer present and the microcontroller clears **GENSTAT**.

The overcurrent filter time is configurable (refer to t_{FOC}) by the control bits OCxFILT(refer to **HBIDIAG**).

t_{FOC} refers to the output of the current sense amplifier. The CSO settling time (2 µs max, t_{SET}) and the analog propagation delay (< 1 µs) are not taken into account by the overcurrent filter time.

7.11.5 CSO outputs capacitor

The capacitor directly connected to CSOx (CCSOx) must be between 10 pF and 400 pF (refer to **Chapter 10**).

The control bit **CCSO** (see **PWM_IDCHG_ACT**, **PWM_PDCHG_INIT**) optimizes the VDD current consumption for CCSOx < 100 pF or CCSOx > 100 pF.

7.12 Electrical characteristics protections and diagnostics

The specified drain-source monitoring thresholds, the overcurrent thresholds and the electrical characteristics related to the current sense amplifiers are valid for $V_{CP} > V_S + 8\ V$

Table 25 Electrical characteristics:

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C
$V_{CP} > V_S + 8\ V$
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Watchdog							
Watchdog period 1	T_{WDPER1}	40	50	60	ms	1) WDPER = 0	P_7.11.52
Watchdog period 2	T_{WDPER2}	160	200	240	ms	1) WDPER = 1	P_7.11.53
Off-state Open load diagnosis							
Pull-up diagnosis current	I_{PUDiag}	-630	-450	-270	µA	1)	P_7.11.1
Pull-down diagnosis current	I_{PDDiag}	900	1250	1600	µA	1)	P_7.11.2
Diagnosis current ratio	I_{Diag_ratio}	2.5	3.0	–		Ratio I_{PDDiag}/I_{PUDiag}	P_7.11.77
Drain source monitoring threshold							
Drain-source monitoring thresholds	$V_{VDSMONTH0}$	0.12	0.15	0.18	V	HBxVDSTH[2:0] = 000_B	P_7.11.3
Drain-source monitoring thresholds	$V_{VDSMONTH1}$	0.16	0.20	0.24	V	HBxVDSTH[2:0] = 001_B	P_7.11.4
Drain-source monitoring thresholds	$V_{VDSMONTH2}$	0.20	0.25	0.30	V	HBxVDSTH[2:0] = 010_B	P_7.11.5
Drain-source monitoring thresholds	$V_{VDSMONTH3}$	0.24	0.30	0.36	V	HBxVDSTH[2:0] = 011_B	P_7.11.6
Drain-source monitoring thresholds	$V_{VDSMONTH4}$	0.32	0.40	0.48	V	HBxVDSTH[2:0] = 100_B	P_7.11.7
Drain-source monitoring thresholds	$V_{VDSMONTH5}$	0.40	0.50	0.62	V	HBxVDSTH[2:0] = 101_B	P_7.11.8
Drain-source monitoring thresholds	$V_{VDSMONTH6}$	0.48	0.60	0.72	V	HBxVDSTH[2:0] = 110_B	P_7.11.9
Drain-source monitoring thresholds	$V_{VDSMONTH7}$	1.6	2.0	2.4	V	HBxVDSTH[2:0] = 111_B	P_7.11.54
Drain-source monitoring blank time							
DS monitoring blank time	t_{DSMON_BLK0}	500	625	850	ns	TBLANKx[2:0] = 000_B 1)	P_7.11.10
DS monitoring blank time	t_{DSMON_BLK1}	0.8	1	1.2	µs	TBLANKx[2:0] = 001_B 1)	P_7.11.11
DS monitoring blank time	t_{DSMON_BLK2}	1	1.25	1.5	µs	TBLANKx[2:0] = 010_B 1)	P_7.11.12

Table 25 Electrical characteristics: (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C
$V_{CP} > V_S + 8$ V
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
DS monitoring blank time	t_{DSMON_BLK3}	1.2	1.5	1.8	µs	TBLANKx[2:0] = 011_B 1)	P_7.11.13
DS monitoring blank time	t_{DSMON_BLK4}	1.6	2	2.4	µs	TBLANKx[2:0] = 100_B 1)	P_7.11.57
DS monitoring blank time	t_{DSMON_BLK5}	2.4	3	3.6	µs	TBLANKx[2:0] = 101_B 1)	P_7.11.58
DS monitoring blank time	t_{DSMON_BLK6}	3.2	4	4.8	µs	TBLANKx[2:0] = 110_B 1)	P_7.11.59
DS monitoring blank time	t_{DSMON_BLK7}	12.8	16	19.2	µs	TBLANKx[2:0] = 111_B 1)	P_7.11.60
Drain-source monitoring filter time							
DS monitoring filter time	t_{DSMON_FILT0}	0.4	0.5	0.85	µs	TFVDS[1:0] = 00_B 1)	P_7.11.14
DS monitoring filter time	t_{DSMON_FILT1}	0.8	1	1.4	µs	TFVDS[1:0] = 01_B 1)	P_7.11.15
DS monitoring filter time	t_{DSMON_FILT2}	1.6	2	2.4	µs	TFVDS[1:0] = 10_B 1)	P_7.11.16
DS monitoring filter time	t_{DSMON_FILT3}	2.4	3	3.6	µs	TFVDS[1:0] = 11_B 1)	P_7.11.17
Cross-current protection time							
Cross current protection time	$t_{HBxCCP0}$	300	375	450	ns	THBxCCP[2:0] = 000_B 1)	P_7.11.18
Cross current protection time	$t_{HBxCCP1}$	500	625	750	ns	THBxCCP[2:0] = 001_B 1)	P_7.11.19
Cross current protection time	$t_{HBxCCP2}$	0.8	1	1.2	µs	THBxCCP[2:0] = 010_B 1)	P_7.11.20
Cross current protection time	$t_{HBxCCP3}$	1.2	1.5	1.8	µs	THBxCCP[2:0] = 011_B 1)	P_7.11.21
Cross current protection time	$t_{HBxCCP4}$	1.6	2	2.4	µs	THBxCCP[2:0] = 100_B 1)	P_7.11.22
Cross current protection time	$t_{HBxCCP5}$	2.4	3	3.6	µs	THBxCCP[2:0] = 101_B 1)	P_7.11.23
Cross current protection time	$t_{HBxCCP6}$	3.2	4	4.8	µs	THBxCCP[2:0] = 110_B 1)	P_7.11.24
Cross current protection time	$t_{HBxCCP7}$	12.8	16	19.2	µs	THBxCCP[2:0] = 111_B 1)	P_7.11.25
Bridge driver passive mode: BD_PASS = 1 and all HBxMODE[1:0] = 00_B or 11_B, or EN = Low or $V_{DD} < V_{DD\ POR}$							

Table 25 Electrical characteristics: (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C
$V_{CP} > V_S + 8$ V
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Passive V_S overvoltage	$V_{SOV\ PASS\ OFF}$	28	31.5	35	V	V_S increasing PASS_MOD=10_B	P_7.11.66
Passive V_S overvoltage hysteresis	$V_{SOV\ PASS\ HY}$	1	2.5	4	V	1)	P_7.11.67
PWM3 open drain resistance	R_{PWM3_OD}	4	5.5	7	kΩ		P_7.11.68
Passive turn-on time	$t_{ON\_BD\_PASS}$	-	4.5	10	µs	1) Cap = 10 nF, VCap = 5 V, VS > 8 V	P_7.11.69
Passive Turn-off time	$t_{OFF\_BD\_PASS}$	-	0.7	2	µs	1) Cap = 10 nF, VCap down to 1.5 V, VS > 8 V	P_7.11.70
Passive LS gate voltage	V_{GLx_BRAKE}	5	–	10	V	VGLx - VSL, x = 1 to 4, VS > 8 V	P_7.11.71
Passive turn-on blank time	$t_{BLK\_BD\_PASS}$	2	6	10	µs	1)	P_7.11.72
PWM1 high voltage, bridge driver passive	$V_{PWM1H\_BD\_PASS}$	0.5	1.3	2.0	V		P_7.11.73
Passive VDS filter time	$t_{DSMON\_FILT\_BD\_PASS}$	0.5	1	2	µs	1)	P_7.11.74
Passive drain-source monitoring thresholds	$V_{VDSMON\_BD\_PASS}$	0.30	0.37	0.44	V	**PASS_VDS**=1_B	P_7.11.75
Current sense amplifier							
Operating common mode input voltage range referred to GND (CSIPx - GND) or (CSINx - GND)	V_{CM}	-2.0	–	28	V		P_7.11.26
Common Mode Rejection Ratio	CMRR	69 75 81 81	– – – –	– – – –	dB	CSAG = (0,0) CSAG = (0,1) CSAG = (1,0) CSAG = (1,1) DC to 50 kHz V_{CM} = -2 … 28 V 1) $V_{CSIPx} = V_{CSINx}$	P_7.11.27
Settling time to 98%	t_{SET}	–	1500	2000	ns	1)	P_7.11.28
Settling time to 98% after gain change	t_{SET_GAIN}	–	–	5000	ns	1) After gain change from CSN rising edge	P_7.11.65
Input Offset voltage	V_{OS}	-1.5	0	1.5	mV		P_7.11.29
Current Sense Amplifier DC Gain (uncalibrated)	G_{DIFF10}	9.9	10	10.1	V/V	CSAG = (0,0)	P_7.11.30

Table 25 Electrical characteristics: (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C
$V_{CP} > V_S + 8$ V
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Sense Amplifier DC Gain (uncalibrated)	G_{DIFF20}	19.8	20	20.2	V/V	CSAG = (0,1)	P_7.11.31
Current Sense Amplifier DC Gain (uncalibrated)	G_{DIFF40}	39.6	40	40.4	V/V	CSAG = (1,0)	P_7.11.32
Current Sense Amplifier DC Gain (uncalibrated)	G_{DIFF80}	79.2	80	80.8	V/V	CSAG = (1,1)	P_7.11.33
Gain drift	G_{DRIFT}	-0.5	–	0.5	%	1) Gain drift after calibration	P_7.11.34
CSOx single ended output voltage range (linear range)	V_{CSOx}	0.5	–	V_{DD} - 0.5	V	1)	P_7.11.35
Reference voltage for unidirectional CSAx	$V_{REF\ Unidir}$	-1%	$V_{DD}/5$	+1%	V	CSDx = 0 $V_{CSIPx} = V_{CSINx}$	P_7.11.36
Reference voltage for bidirectional CSAx	$V_{REF\ Bidir}$	-1%	$V_{DD}/2$	+1%	V	CSDx = 1 $V_{CSIPx} = V_{CSINx}$	P_7.11.37
Overcurrent detection							
Overcurrent filter time	t_{FOC}	4 7 40 85	6 10 50 100	8 13 60 115	µs	OCxFILT = 00_B OCxFILT = 01_B OCxFILT = 10_B OCxFILT = 11_B 1)2)	P_7.11.38
OC threshold, unidirectional	$V_{OCTH1\ Unidir}$	-4%	$V_{DD}/2$	+4%	V	CSDx = 0, OCTH[1:0]= 00_B	P_7.11.39
OC threshold, unidirectional	$V_{OCTH2\ Unidir}$	-4%	$V_{DD}/2 + V_{DD}/10$	+4%	V	CSDx = 0, OCTH[1:0]= 01_B	P_7.11.40
OC threshold, unidirectional	$V_{OCTH3\ Unidir}$	-4%	$V_{DD}/2 + 2x\ V_{DD}/10$	+4%	V	CSDx = 0, OCTH[1:0]= 10_B	P_7.11.41
OC threshold, unidirectional	$V_{OCTH4\ Unidir}$	-4%	$V_{DD}/2 + 3x\ V_{DD}/10$	+4%	V	CSDx = 0, OCTH[1:0]= 11_B	P_7.11.42
High OC threshold, bidirectional	$V_{OCTH1\ BidirH}$	-4%	$V_{DD}/2 + 2x\ V_{DD}/20$	+4%	V	CSDx = 1, OCTH[1:0]= 00_B	P_7.11.43
High OC threshold, bidirectional	$V_{OCTH2\ BidirH}$	-4%	$V_{DD}/2 + 4x\ V_{DD}/20$	+4%	V	CSDx = 1, OCTH[1:0]= 01_B	P_7.11.44
High OC threshold, bidirectional	$V_{OCTH3\ BidirH}$	-4%	$V_{DD}/2 + 5x\ V_{DD}/20$	+4%	V	CSDx = 1, OCTH[1:0]= 10_B	P_7.11.45

Table 25 Electrical characteristics: (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C
$V_{CP} > V_S + 8$ V
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High OC threshold, bidirectional	$V_{OCTH4\ BidirH}$	-4%	$V_{DD}/2$ + 6x $V_{DD}/20$	+4%	V	CSDx = 1, OCTH[1:0]= 11_B	P_7.11.46
Low OC threshold, bidirectional	$V_{OCTH1\ BidirL}$	-4%	$V_{DD}/2$ - 2x $V_{DD}/20$	+4%	V	CSDx = 1, OCTH[1:0]= 00_B	P_7.11.61
Low OC threshold, bidirectional	$V_{OCTH2\ BidirL}$	-4%	$V_{DD}/2$ - 4x $V_{DD}/20$	+4%	V	CSDx = 1, OCTH[1:0]= 01_B	P_7.11.62
Low OC threshold, bidirectional	$V_{OCTH3\ BidirL}$	-4%	$V_{DD}/2$ - 5x $V_{DD}/20$	+4%	V	CSDx = 1, OCTH[1:0]= 10_B	P_7.11.63
Low OC threshold, bidirectional	$V_{OCTH4\ BidirL}$	-4%	$V_{DD}/2$ - 6x $V_{DD}/20$	+4%	V	CSDx = 1, OCTH[1:0]= 11_B	P_7.11.64
Thermal warning and shutdown							
Thermal warning junction temperature	T_{jW}	120	140	160	°C	See **Figure 36**[1]	P_7.11.48
Thermal shutdown junction temperature	T_{jSD}	160	180	200	°C	See **Figure 36**[1]	P_7.11.49
Thermal shutdown hysteresis	T_{jHYS}	–	10	–	°C	[1]	P_7.11.50
Ratio of T_{jSD} to T_{jW}	T_{jSD}/T_{jW}	–	1.20	–	–	[1]	P_7.11.51
Thermal warning filter time	t_{jW_FILT}	7	10	13	µs	[1]	P_7.11.55
Thermal shutdown filter time	t_{jSD_FILT}	7	10	13	µs	[1]	P_7.11.56

1) Not subject to production test, specified by design.

2) t_{FOC} refers to the output of the current sense amplifier. The CSO settling time (2 µs max, t_{SET}) and the analog propagation delay (< 1 µs)are not taken into account by the overcurrent filter time.

8 Serial Peripheral Interface - SPI

The 24-bit Serial Peripheral Interface (SPI) enables the communication between the microcontroller and the TLE92104-232. It allows to configure and control the device, and to read out the status registers for diagnostic purpose.The MOSFET driver IC acts as a SPI-slave while the microcontroller acts as a SPI-master.

The interface has a serial data input pin (SDI) to transfer data to the device, a serial data output pin (SDO) for reading data back from the device, and a serial clock pin (SCLK) for clocking data into and out of the device. A chip select pin (CSN) enables or disables the serial interface.

The SPI frame starts with the falling edge of CSN. During the falling edge of CSN, SCLK must be low (Clock Polarity CPOL = 0). Received data on SDI are shifted in on the falling edge of SCLK. Transmitted data by SDO are shifted out on the rising edge of SCLK (Clock Phase CPHA = 1). Refer to **Figure 42**.

The Most Significant Bit (MSB, bit 23) is shifted in/out first.

Write and clear commands are executed at the rising edge of CSN.

The SPI protocol supports both independent slave selection and daisy chain configurations.

8.1 SPI protocol with independent slave selection

With individual slave selection, the microcontroller controls the CSN pin of each SPI slave individually (**Figure 41**).

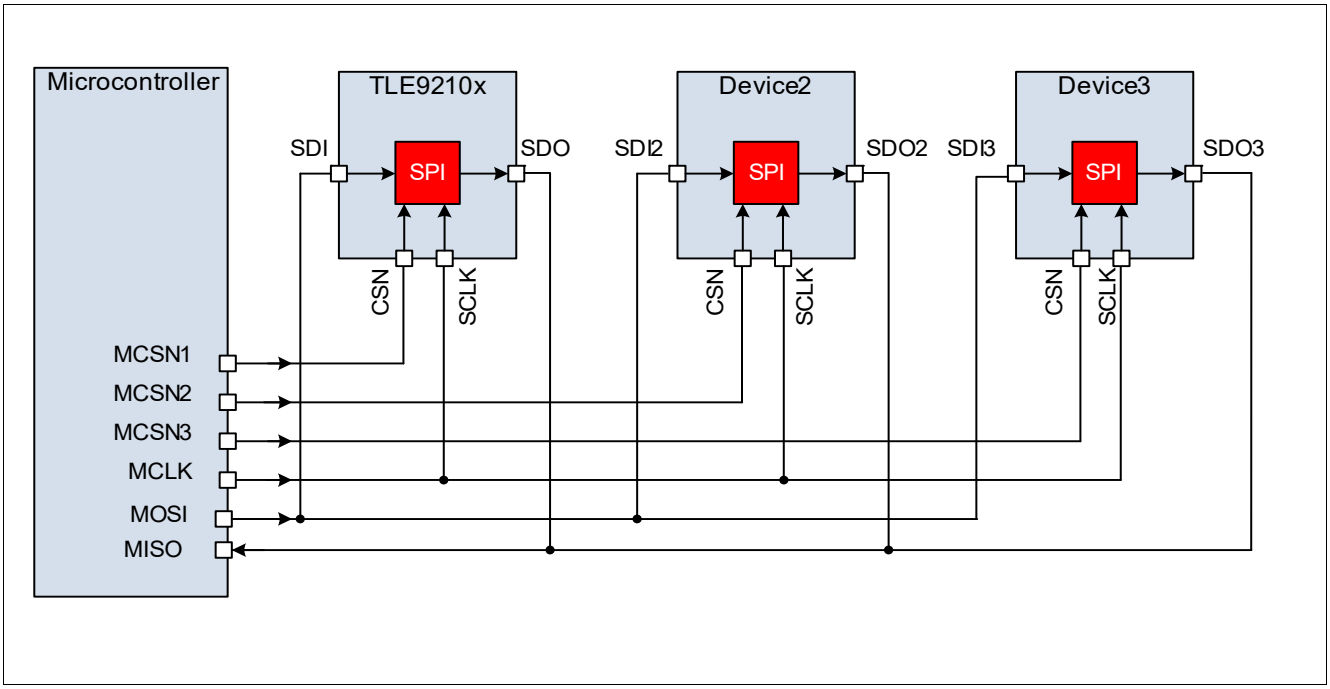


Figure 41 Individual slave selection with three slave devices

A SPI communication consists of 24-bit frame (**Figure 42**):

- SDI receives one address byte followed by two data bytes.
- SDO transmits the Global Error Flag and the Global Status Byte followed by two response bytes.

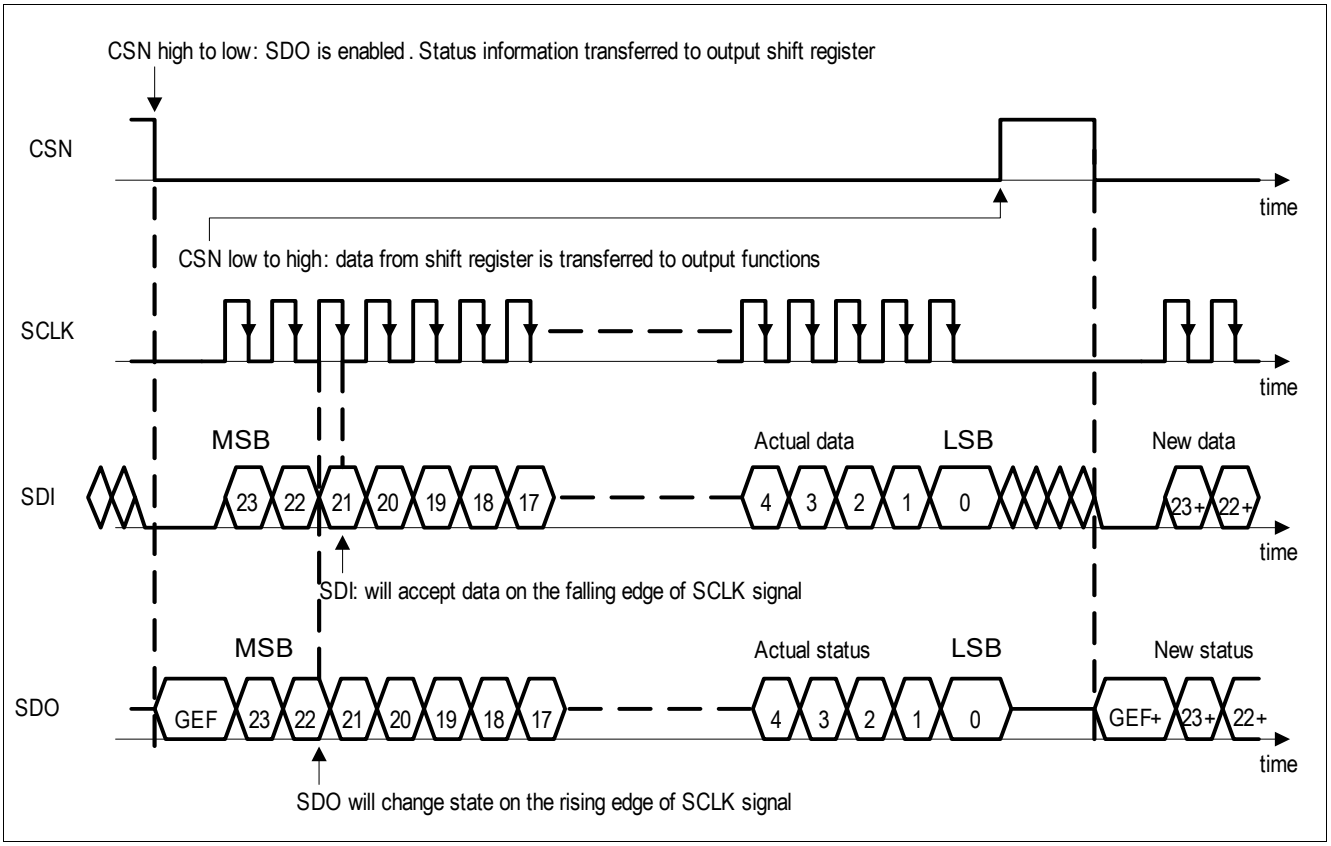


Figure 42 SPI Data Transfer

The MSB of the address byte must be set to '1'.

The address byte specifies (see **Figure 43**):

- the target register (A[4:0])
- the type of operation:
  - For control registers:
  - Read only: OP bit[1] = '0'
  - Read and write: OP bit = '1'
  - For status registers:
  - Read only: OP bit = '0'
  - Read and clear: OP bit = '1'

With individual slave selection, the Last Address Byte Token (LABT) must be set to '1'.

In-frame response

The SPI protocol incorporates an in-frame response: The content of the addressed register is shifted out by SDO within the same SPI frame. This feature reduces the SPI bus load during the read out of the control or status registers.

1) OP bit is the least significant bit of the address byte, see **Figure 43**

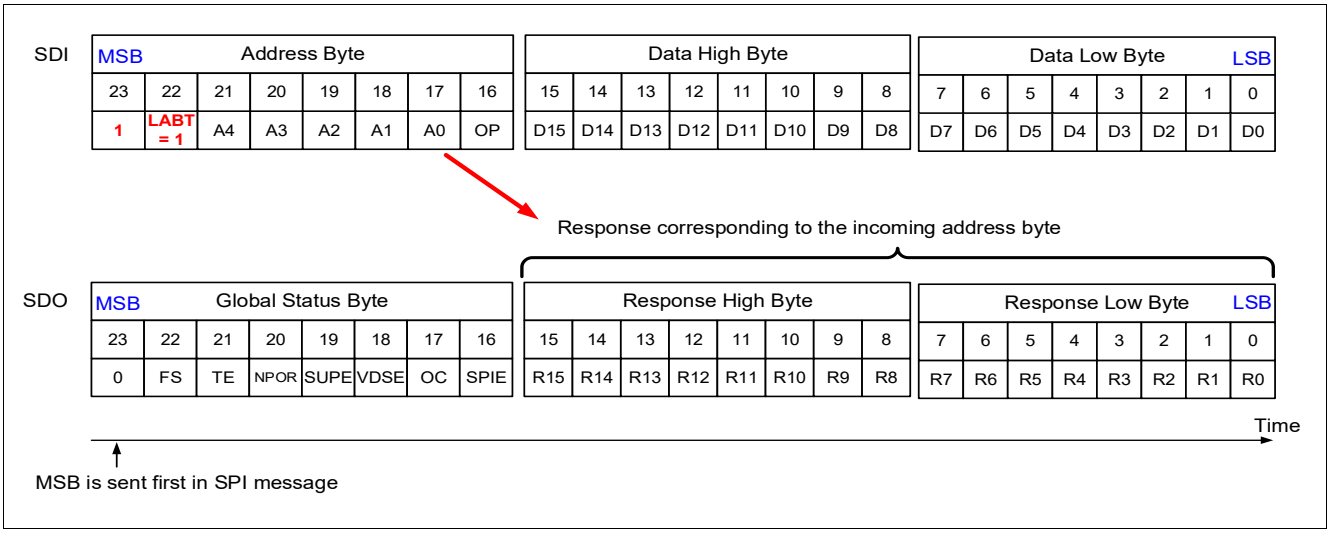


Figure 43 In-frame response with individual slave selection

8.2 Global Error Flag (GEF)

The Global Error Flag (GEF) is reported on SDO between the CSN falling edge and the first SCLK rising edge. GEF is set if a fault condition is detected or if the device comes from a Power On Reset (POR). It is therefore possible to have a quick device diagnostic without any SPI clock pulse (**Figure 44**).

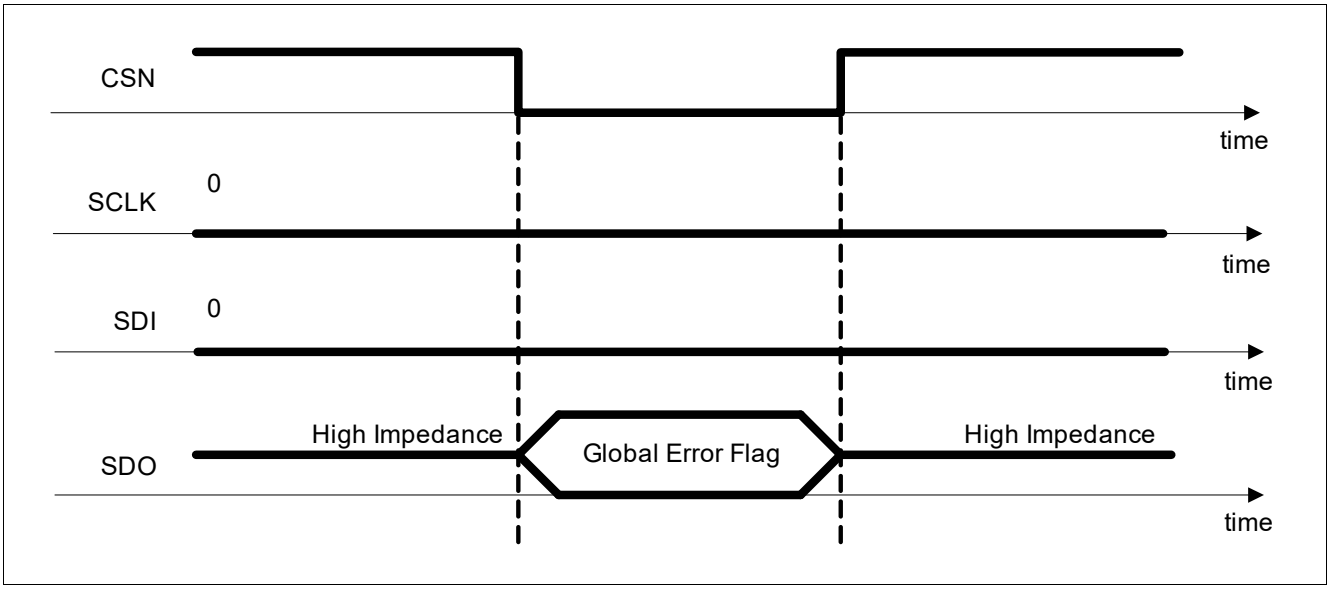


Figure 44 GEF - Diagnostic with 0-clock cycle

8.3 Global status byte

The SDO shifts out during the first eight SCLK cycles the Global Status Byte. This register provides an overview of the device status. The following error conditions are reported in this byte:

- Fail Safe (FS bit).
- Temperature error (TE bit): logical OR combination between Thermal Warning (**TW**) and Thermal shutdown (**TSD**).
- **Negated** Power ON Reset (NPOR bit, refer to **Chapter 5.3** for reset conditions).

- Supply Error (SUPE bit): logical OR combination between VS undervoltage shutdown (**VSUV**), VS overvoltage shutdown (**VSOV**) and charge pump undervoltage (**CPUV**).
- VDS monitoring Error (VDSE bit): logical OR combination between the bits of the **DSOV** register.
- Overcurrent (OC bit): logical OR combination between OC1 and OC2 status bits (**GENSTAT** register).
- SPI protocol Error (SPIE bit).

*Note: The Global Error Flag is a logic OR combination of every bit of the Global Status Byte and of TDREGx: GEF = (FS) OR (TE) OR (**NOT(NPOR)**) OR (SUPE) OR (VDSE) OR (OC) OR (SPIE) OR **(NOT(TDREGx) AND (PWMx_EN =1) AND (NOT (MSKTDREG)))**, x = 1 ... 3.*

The following table shows how failures are reported in the Global Status Byte and the error Flag:

Table 26 Failure reported in the global status byte and global error flag

Type of Error	Failure reported in the Global Status Byte	Global Error Flag
Fail safe	FS = 1	1
Thermal error	TE = 1	1
Power ON reset	**NPOR = 0**	1
Supply error	SUPE = 1	1
Drain source voltage monitoring	VDSE = 1	1
Overcurrent	OC = 1	1
SPI protocol error	SPIE = 1	1
TDREGx, x = 1 ... 3[1] (see **GENSTAT**)	-	1 if MSKTDREG = 0[2] 0 if MSKTDREG = 1[2]
No error and no power ON reset	SPIE = 0 OC = 0 VDSE = 0 SUPE= 0 **NPOR = 1** TE = 0 FS = 0 TDREGx = 0,	0

1) See status register **GENSTAT**.
2) See control register **GENCTRL2**.

Note: The default value (after Power ON Reset) of NPOR is 0, therefore the default value of GEF is 1.

In fail safe mode, the control registers are frozen to their default value, with the exception of the WDTRIG bit (refer to **Chapter 5.2.3**). Any write access (except for WDTRIG bit) in fail safe mode will be discarded and the SPIE bit will set.

8.4 SPI error detection

The SPI incorporates an error flag in the Global Status Byte (SPIE) to supervise and preserve the data integrity. If an SPI protocol error is detected during a given frame, the SPIE bit is set in the next SPI communication.

The SPIE bit is set in the following error conditions:

- The number of SCLK clock pulses received when CSN is Low is (protocol error):
  - not zero
  - or less than 24
  - or more than 24 but not a multiple of 8
- The microcontroller sends an SPI command to an unused address (protocol error).
- A clock polarity error is detected (see **Figure 45** Case 2 and Case 3): the incoming clock signal was High during CSN rising or falling edges (protocol error).
- No address byte or no last address byte are detected (protocol error).
- In daisy chain: the microcontroller does not send in sequence the first address byte until the last address byte (i.e. with gaps between two address bytes). In this case, the SDO signal is set to '0' during the remaining part of the SPI frame[1)], in order to prevent other devices from executing wrong commands (protocol error).
- A clear command to address 0x1F (Device ID register, Offset address = 0x1F).
- The same half-bridge is allocated to several activated PWM channels.
- Any write or clear command received in fail safe mode and not belonging to the exit sequence (refer to **Chapter 5.2.3**).

Note: SPI commands to activate a half-bridge mapped to several PWM channels are ignored.

In fail safe mode, the control registers may not be accessed, except for writing WDTRIG. An invalid write command in this mode sets the SPIE bit.

For a correct SPI communication:

- SCLK must be Low for a minimum t_{BEF} before CSN falling edge and t_{lead} after CSN falling edge.
- SCLK must be Low for a minimum t_{lag} before CSN rising edge and t_{BEH} after CSN rising edge.

1) Provided that the SPI frame has a correct polarity

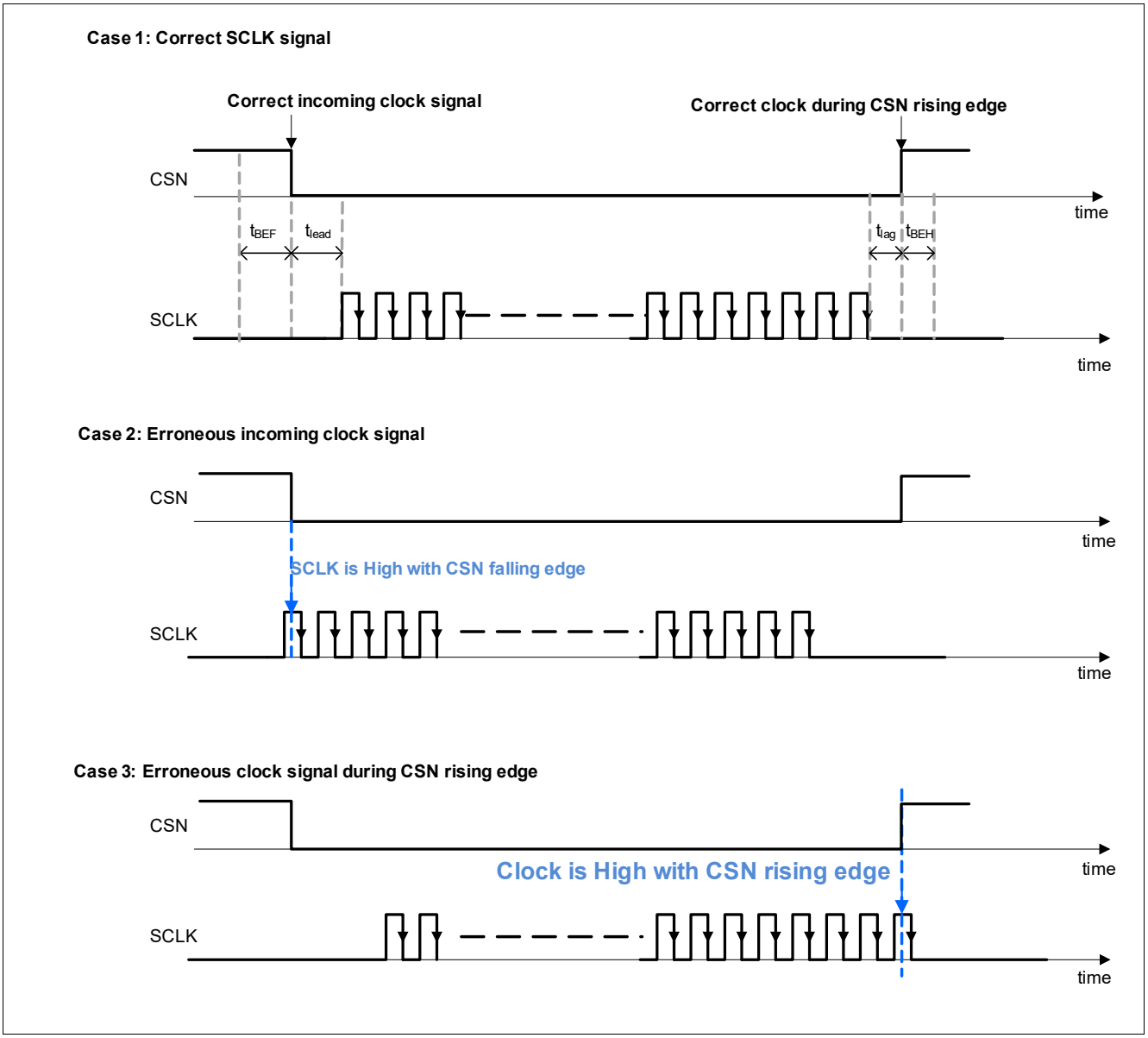


Figure 45 Clock polarity error

The reset condition of the SPIE bit depends on the cause of error:

- In normal mode:
  - The microcontroller must clear **HBVOUT_PWMERR** if one half-bridge has been allocated to several PWM channels.
  - The microcontroller must send a correct SPI frame for the other errors reported by SPIE.
- If SPIE has been set in fail safe mode, the device must enter normal mode first.

8.5 Daisy chain

In daisy chain configuration the master output / slave input (noted MOSI) is connected to a slave SDI. The first slave SDO is connected to the next slave SDI in the chain. The SDO of the final in the chain is connected to the master input / slave output (noted MISO). In daisy chain configuration, the microcontroller MCSN is connected to all the slave CSN inputs (**Figure 46**).

To support daisy chain configurations, the TLE92104-232 accepts SPI frames with more than 24 bits, provided that the number of bits is a multiple of 8, and the structure of the address byte is respected.

In daisy chain, the TLE92104-232 works as follows:

1. The TLE92104-232 operates as a 8-bit shift register until it receives the first address byte. This first received address byte is considered by the device as its own address byte.
2. The TLE92104-232 copies directly SDI to SDO until the last address byte is detected.
3. The TLE92104-232 shifts out the response high byte and low byte corresponding to the address byte.
4. After the last address byte, the TLE92104-232 operates as a 16-bit shift register until the end of the SPI frame.

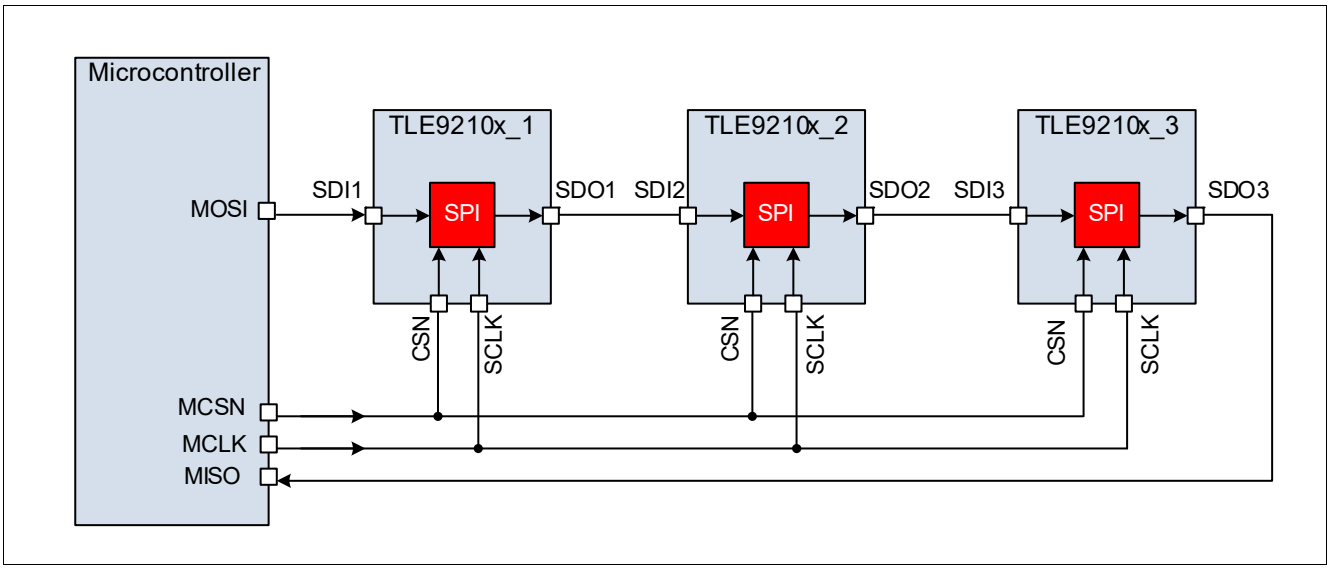


Figure 46 Daisy chain configuration with three TLE9210x devices

In daisy chain configuration (**Figure 46**), the microcontroller must send the address and data bytes in the following order (**Figure 47**):

1. The address bytes altogether are sent first:
   - Address byte 1 (for TLE9210x_1) is sent first, followed by address byte 2 (for TLE9210x_2), followed by address byte 3 (for TLE9210x_3).
   - The LABT bit of the last address byte must be '1', while the LABT bit of all the other address bytes must be '0'.
2. The data bytes are sent altogether **in reverse order** once the address bytes are transmitted:
   - The data high byte for the TLE9210x_3 is sent first followed by the data low byte for the TLE9210x_3.
   - Then the data high byte for the TLE9210x_2 is sent followed by the data low byte for the TLE9210x_2.
   - Then the data high byte for the TLE9210x_1 is sent followed by the data low byte for the TLE9210x_1.

The Master Input / Slave Output (MISO), which is connected to SDO of the last device in the daisy chain, receives:

1. A logic OR combination of all Global Error Flags (GEF) at the beginning of the SPI frame, between CSN falling edge and the first SCLK rising edge.
2. The Global Status Byte of each TLE9210x **in reverse order**:

- The Global Status Byte 3 (GSB3) corresponding to the TLE9210x_3 is received first, followed by GSB2 (corresponding to the TLE9210x_2), and finally the GSB1 (corresponding to the TLE9210x_1) is received.

3. The response of each TLE9210x **in reverse order**:
   - The response high byte of the TLE9210x_3 is received first followed by the response low byte of the TLE9210x_3.
   - Then the response high byte of the TLE9210x_2 is received followed by the response low byte of the TLE9210x_2.
   - Then the response high byte of the TLE9210x_1 is received followed by the response low byte of the TLE9210x_1.

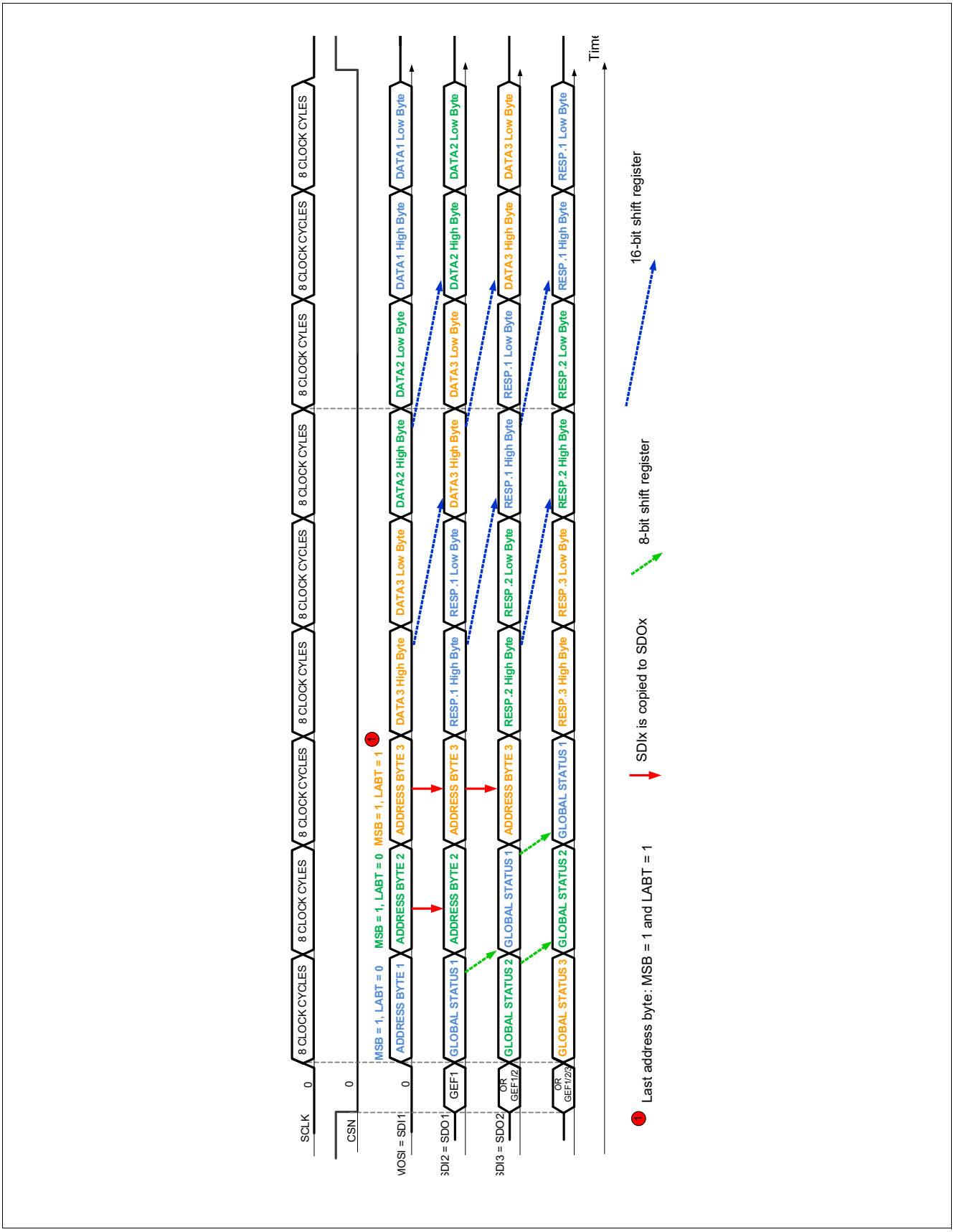


Figure 47 SPI Frame in daisy chain configuration with three TLE9210x devices

8.6 SPI electrical characteristics: timings

Table 27 Electrical characteristics: SPI interface

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	4	MHz	1)	P_8.6.1
Delay from EN rising edge to first SPI frame							
SPI interface setup time2)	t_{SET_SPI}	–	–	150	µs	1)	P_8.6.32
SPI interface, logic inputs SDI, SCLK, CSN							
High input voltage threshold	V_{IH}	0.7 x V_{DD}	–	–	V		P_8.6.2
Low input voltage threshold	V_{IL}	–	–	0.3 x V_{DD}	V		P_8.6.3
Hysteresis of input voltage	V_{IHY}	–	0.12 x V_{DD}	–	V	1)	P_8.6.4
Pull up resistor at pin CSN	R_{PU_CSN}	20	40	80	kΩ	V_{CSN} = 0.7 x V_{DD}	P_8.6.5
Pull down resistor at pin SDI, SCLK	R_{PD_SDI}, R_{PD_SCLK}	20	40	80	kΩ	V_{SDI}, V_{SCLK} = 0.2 x V_{DD}	P_8.6.6
Input capacitance at pin CSN, SDI or SCLK	C_I	–	10	–	pF	1) 0 V < V_{DD} < 5.5 V	P_8.6.7
Input interface, logic outputs SDO							
H-output voltage level	V_{SDOH}	0.8 x V_{DD}	–	–	V	I_{SDOH} = -1.6 mA	P_8.6.8
L-output voltage level	V_{SDOL}	–	–	0.2 x V_{DD}	V	I_{SDOL} = 1.6 mA	P_8.6.9
Tri-state Leakage Current	I_{SDOLK}	-10	–	10	µA	1) V_{CSN} = V_{DD}; 0 V < V_{SDO} < V_{DD}	P_8.6.10
Tri-state input capacitance	C_{SDO}	–	10	15	pF	1)	P_8.6.11
Data input timing. See Figure 41							
SCLK Period	t_{pCLK}	250	–	–	ns	1)	P_8.6.12
SCLK High Time	t_{SCLKH}	0.45 x t_{pCLK}	–	0.55 x t_{pCLK}	ns	1)	P_8.6.13
SCLK Low Time	t_{SCLKL}	0.45 x t_{pCLK}	–	0.55 x t_{pCLK}	ns	1)	P_8.6.14
SCLK Low before CSN Low	t_{BEF}	125	–	–	ns	1)	P_8.6.15
CSN Setup Time	t_{lead}	250	–	–	ns	1)	P_8.6.16
SCLK Setup Time	t_{lag}	250	–	–	ns	1)	P_8.6.17
SCLK Low after CSN High	t_{BEH}	125	–	–	ns	1)	P_8.6.18
SDI Setup Time	t_{SDI_setup}	100	–	–	ns	1)	P_8.6.19

Table 27 Electrical characteristics: SPI interface (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SDI Hold Time	t_{SDI_hold}	50	–	–	ns	1)	P_8.6.20
Input Signal Rise Time at pin SDI, SCLK, CSN	t_{rIN}	–	–	50	ns	1)	P_8.6.21
Input Signal Fall Time at pin SDI, SCLK, CSN	t_{fIN}	–	–	50	ns	1)	P_8.6.22
Delay time from EN falling edge to standby mode	t_{DMODE}	–	–	6	µs	1)	P_8.6.23
Minimum CSN High Time	t_{CSNH}	3	–	–	µs	1)	P_8.6.24
Data output timing. See Figure 42.							
SDO Rise Time	t_{rSDO}	–	30	80	ns	1) C_{load} = 100 pF	P_8.6.25
SDO Fall Time	t_{fSDO}	–	30	80	ns	1) C_{load} = 100 pF	P_8.6.26
SDO Enable Time after CSN falling edge	t_{ENSDO}	–	–	50	ns	1) Low Impedance	P_8.6.27
SDO Disable Time after CSN rising edge	t_{DISSDO}	–	–	50	ns	1) High Impedance	P_8.6.28
Duty cycle of incoming clock at SCLK	$duty_{SCLK}$	45	–	55	%	1)	P_8.6.29
SDO Valid Time for V_{DD} = 5V	t_{VASDO5}	–	–	50	ns	1) V_{SDO} < 0.2 x V_{DD} V_{SDO} > 0.8 x V_{DD} C_{load} = 100 pF	P_8.6.31

1) Not subject to production test, specified by design

2) Delay required between EN rising edge and the moment when the device can accept SPI commands

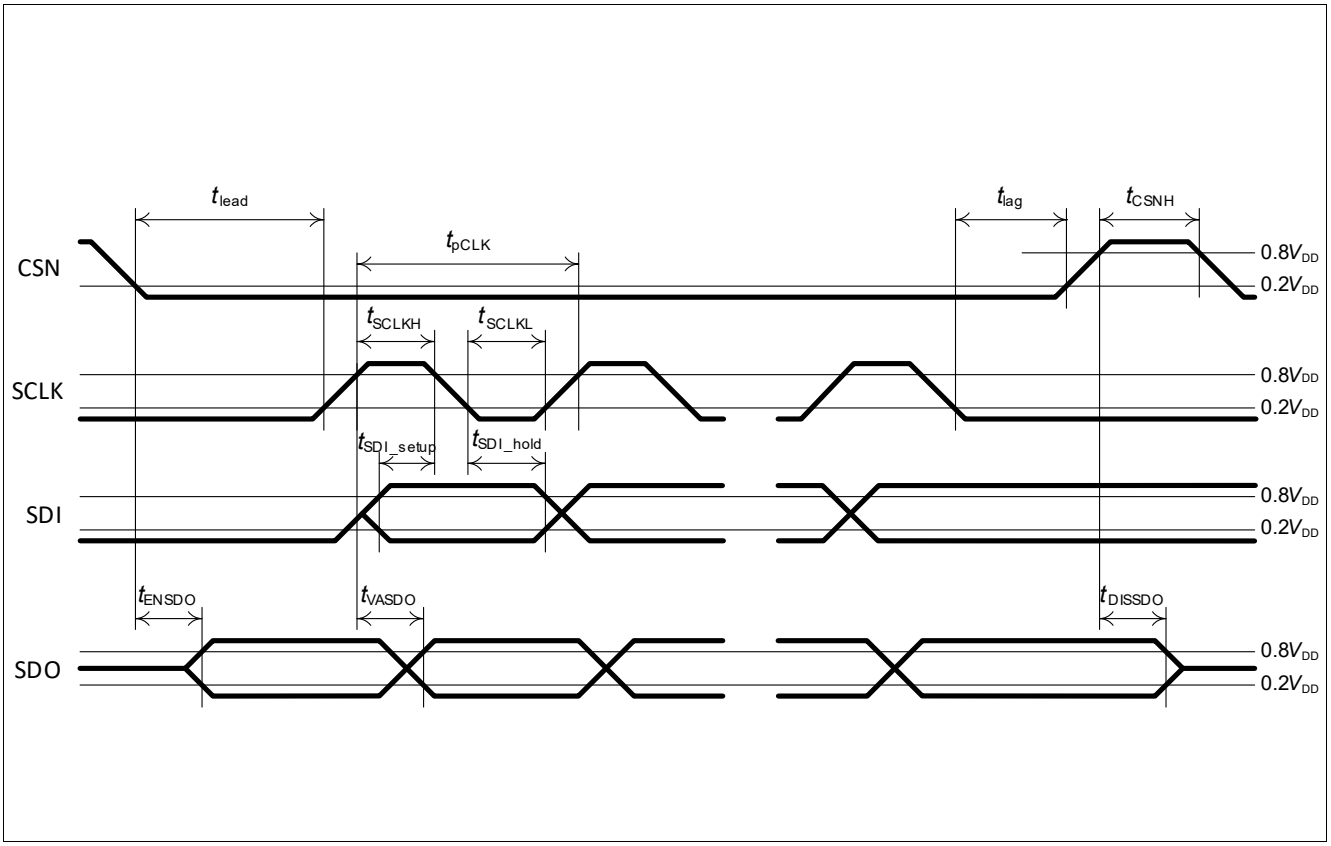


Figure 48 SPI timing parameters

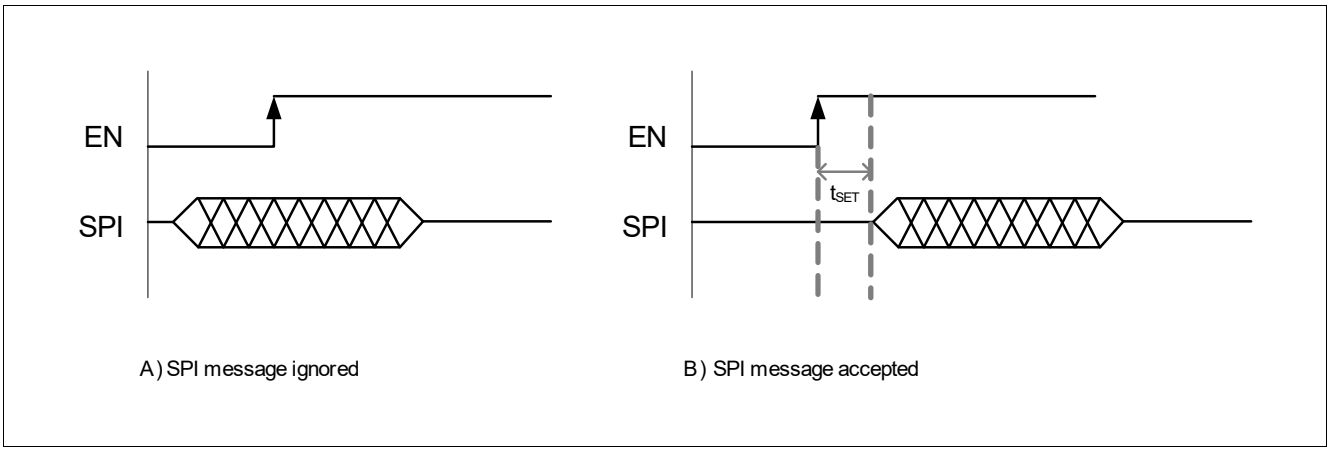


Figure 49 Setup time from EN rising edge to first SPI communication

9 Register specification

9.1 Control registers

Table 28 Register Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
GENCTRL1	General control register 1	0x00 and REG_BANK = 0 or 1	0x0026
GENCTRL2	General control register 2	0x01 and REG_BANK = 0 or 1	0x4180
VDS1	Drain-source monitoring HB1-4	0x02 and REG_BANK = 0 or 1	0x0249
CCP_BLK1	Cross current protection and blank times setting 1	0x04 and REG_BANK = 0 or 1	0x0000
CCP_BLK2_ACT	Cross current protection and blank times setting **for active MOSFETs**[1)]	0x05 and REG_BANK = 0	0x4924
CCP_BLK2_FW	Cross current protection and blank times setting **for FW MOSFETs**[1)]	0x05 and REG_BANK = 1	0x4924
HBMODE	Half-bridge mode	0x06 and REG_BANK = 0 or 1	0x0000
PWMSET	Setting of PWM channels	0x07 and REG_BANK = 0	0x6420
TPRECHG	PWM pre-charge and pre-discharge time	0x08 and REG_BANK = 0 or 1	0x0000
HBIDIAG	Half-bridge diagnostic current control	0x09 and REG_BANK = 0 or 1	0xC000
ST_ICHG	Charge current for static half-bridges	0x0A and REG_BANK = 0	0x0044
PWM_PCHG_INIT	Precharge current initialization	0x0A and REG_BANK = 1	0x18C6
PWM_ICHG_ACT	Charge current for half-bridges in PWM **(active MOSFETs[1)])**	0x0B and REG_BANK = 0	0x18C6
PWM_ICHG_FW	Charge current for half-bridges in PWM **(FW MOSFETs[1)]**)	0x0B and REG_BANK = 1	0x18C6
PWM_IDCHG_ACT	Discharge current of **active MOSFETs[1)]** in PWM operation	0x0C and REG_BANK = 0	0x1CE7
PWM_PDCHG_INIT	Predischarge current initialization	0x0C and REG_BANK = 1	0x318C
PWM_ICHGMAX_CCP_BLK3_ACT	Max. pre-charge / pre-discharge currents for half-bridges in PWM[2)], **tCCP and tBLANK setting for active MOSFETS**[1)]	0x0D and REG_BANK =0	0x4900
PWM_ICHGMAX_CCP_BLK3_FW	Max. pre-charge / pre-discharge currents for half-bridges in PWM[2)], **tCCP and tBLANK setting for FW MOSFETS**[1)]	0x0D and REG_BANK =1	0x4900
TDON_OFF1	Turn-on and turn-off delays for PWM channel1	0x0E and REG_BANK = 0 or 1	0x0A0A

Table 28 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
TDON_OFF2	Turn-on and turn-off delays for PWM channel2	0x0F and **REG_BANK** = 0 or 1	0x0A0A
TDON_OFF3	Turn-on and turn-off delays for PWM channel3	0x10 and **REG_BANK** = 0 or 1	0x0A0A

1) Refer to **Chapter 6.3.1** for the definition of the active and the free-wheeling MOSFETs, depending on the setting of **AGC**

2) ICHGMAX is also the current applied to the Active MOSFET during post-discharge.

9.1.1 General Control Registers and Protection Settings

General control register 1

GENCTRL1
General Control Register 1 (0 0000$_B$)Reset Value: 0000 0000 0010 0110$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSD2	CSAG2		CSD1	CSAG1		REG_BANK	VSOVTH	UNLOCK	Reserved	FMODE	Reserved	IPCHGADT	OCEN	WDPER	WDTRIG
rw	rw		rw	rw		rw	rw	rw	r	rw	r	rw	rw	rw	rw

Field	Bits	Type	Description
CSD2	15	rw	**Direction of the current sense amplifier 2** 0_B The current sense is unidirectional (default) 1_B The current sense is bidirectional
CSAG2	14:13	rw	**Gain of the current sense amplifier 2** 00_B 10 V/V (default) 01_B 20 V/V 10_B 40 V/V 11_B 80 V/V
CSD1	12	rw	**Direction of the current sense amplifier 1** 0_B The current sense is unidirectional (default) 1_B The current sense is bidirectional
CSAG1	11:10	rw	**Gain of the current sense amplifier 1** 00_B 10 V/V (default) 01_B 20 V/V 10_B 40 V/V 11_B 80 V/V
REG_BANK	9	rw	**Register banking** 0_B (Default) refer to **CCP_BLK2_ACT**, **PWM_ICHGMAX_CCP_BLK3_ACT**, **PWM_ICHG_ACT**, **ST_ICHG**, **PWM_IDCHG_ACT** , **PWMSET** 1_B Refer to **CCP_BLK2_FW**, **PWM_ICHGMAX_CCP_BLK3_FW**, **PWM_ICHG_FW**,**PWM_PDCHG_INIT**,**PWM_PCHG_INIT**
VSOVTH	8	rw	**VS Overvoltage threshold** 0_B $V_{SOV\ OFF} = V_{SOV\ OFF1}$ (min. 19 V, default) 1_B $V_{SOV\ OFF} = V_{SOV\ OFF2}$ (min. 29V)
UNLOCK	7	rw	**Unlock bit to disable the watchdog** 0_B WDDIS cannot be reset (default) 1_B WDDIS (**GENCTRL2**) can be reset in the following SPI frame
Reserved	6	r	**Reserved. Always read as '0'**
FMODE	5	rw	**Frequency modulation** 0_B No modulation 1_B Modulation frequency 15.6 kHz (default)
Reserved	4	r	**Reserved. Always read as '0'**

Field	Bits	Type	Description
IPCHGADT	3	rw	**Adaptation of the pre-charge and pre-discharge current** 0_B 1 current step (default) 1_B 2 current steps
OCEN	2	rw	**Overcurrent shutdown Enable** 0_B Disabled 1_B Enabled (default)
WDPER	1	rw	**Watchdog period** 0_B 50 ms 1_B 200 ms (default)
WDTRIG	0	rw	**Watchdog trigger bit** This bit must be inverted within a watchdog period. After power on reset, the default value is 0.

Attention: ***Any write access to this register must invert the WDTRIG bit. Otherwise, the device enters fail safe mode. Refer to Chapter 5.2.3.***

General control register 2

GENCTRL2
General Control Register 2 (0 0001$_B$)Reset Value: 0100 0001 1000 0000$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POCHGDIS	BD_PASS	AGCFILT	AGC		IHOLD	WDDIS	MSKTDREG	CPUVTH	CPSTGA	TFVDS		OCTH2		OCTH1	
rw	rw	rw	rw		rw	rw	rw	rw	rw	rw		rw		rw	

Field	Bits	Type	Description
POCHGDIS	15	rw	**Postcharge disable bit** 0_B The postcharge phase is enabled during PWM (default) 1_B The postcharge phase is disabled during PWM
BD_PASS	14	rw	**Bridge driver passive mode** 0_B Bridge driver is in active mode 1_B Bridge driver is in passive mode (Default)
AGCFILT	13	rw	**Filter for adaptive gate control** *Note: Refer to **Adaptive control of pre-charge current** and **Adaptive control of pre-discharge current*** 0_B No filter applied (default) 1_B Filter applied
AGC	12:11	rw	**Adaptive gate control** 00_B (default) Adaptive gate control disabled, pre-charge and pre-discharge disabled 01_B Adaptive gate control disabled, precharge is disabled, predischarge is enabled with IPREDCHG = IPDCHGINIT (Refer to **PWM_PCHG_INIT**) 10_B Adaptive gate control enabled, IPRECHG and IPREDCHG are self adapted 11_B Reserved. Adaptive gate control enabled, IPRECHG and IPREDCHG are self adapted
IHOLD	10	rw	**Gate driver hold current IHOLD** 0_B (default) Charge: I_{CHG8} (12.5 mA typ.), discharge I_{DCHG8} (14.2 mA typ.) 1_B Charge: I_{CHG12} (23.9 mA typ.), discharge: I_{DCHG12} (26.0 mA typ.)
WDDIS	9	rw	**Watchdog disable bit** 0_B the watchdog is enabled (default) 1_B the watchdog is disabled if the previous SPI frame has set UNLOCK bit (**GENCTRL1**) Once the watchdog is disabled, it is directly re-enabled by resetting WDDIS

Field	Bits	Type	Description
MSKTDREG	8	rw	**Masking of the turn-on/off delay error in the Global Error Flag** 0_B Turn-on/off delay error is reported in the GEF 1_B Turn-on/off delay error is masked in the GEF (default)
CPUVTH	7	rw	**Charge pump undervoltage detection threshold** 0_B V_{CPUV} (referred to VS) = 6.0V typ. 1_B V_{CPUV} (referred to VS)= 7.5 V typ. (default)
CPSTGA	6	rw	**Automatic switch-over between dual and single charge pump stage** 0_B Automatic switch over deactivated (default) 1_B Automatic switch over activated
TFVDS	5:4	rw	**Filter time of drain-source voltage monitoring** 00_B 0.5 µs (default) 01_B 1 µs 10_B 2 µs 11_B 3 µs
OCTH2	3:2	rw	**Overcurrent detection threshold of CSO2 with CSD2 = 0** 00_B $V_{CSO2} > V_{DD/2}$(default) 01_B $V_{CSO2} > V_{DD/2} + V_{DD}/10$ 10_B $V_{CSO2} > V_{DD/2} + 2 \times V_{DD}/10$ 11_B $V_{CSO2} > V_{DD/2} + 3 \times V_{DD}/10$ **Overcurrent detection threshold of CSO2 with CSD2 = 1** 00_B $V_{CSO2} > V_{DD/2} + 2 \times V_{DD}/20$ or $V_{CSO2} < V_{DD/2} - 2 \times V_{DD}/20$ (default) 01_B $V_{CSO2} > V_{DD/2} + 4 \times V_{DD}/20$ or $V_{CSO2} < V_{DD/2} - 4 \times V_{DD}/20$ 10_B $V_{CSO2} > V_{DD/2} + 5 \times V_{DD}/20$ or $V_{CSO2} < V_{DD/2} - 5 \times V_{DD}/20$ 11_B $V_{CSO2} > V_{DD/2} + 6 \times V_{DD}/20$ or $V_{CSO2} < V_{DD/2} - 6 \times V_{DD}/20$
OCTH1	1:0	rw	**Overcurrent detection threshold of CSO1 with CSD1 = 0** 00_B $V_{CSO1} > V_{DD/2}$ (default) 01_B $V_{CSO1} > V_{DD/2} + V_{DD}/10$ 10_B $V_{CSO1} > V_{DD/2} + 2 \times V_{DD}/10$ 11_B $V_{CSO1} > V_{DD/2} + 3x\ V_{DD}/10$ **Overcurrent detection threshold of CSO1 with CSD1 = 1** 00_B $V_{CSO1} > V_{DD/2} + 2 \times V_{DD}/20$ or $V_{CSOx} < V_{DD/2} - 2x\ V_{DD}/20$ (default) 01_B $V_{CSO1} > V_{DD/2} + 4x\ V_{DD}/20$ or $V_{CSOx} < V_{DD/2} - 4x\ V_{DD}/20$ 10_B $V_{CSO1} > V_{DD/2} + 5 \times V_{DD}/20$ or $V_{CSOx} < V_{DD/2} - 5 \times V_{DD}/20$ 11_B $V_{CSO1} > V_{DD/2} + 6x\ V_{DD}/20$ or $V_{CSOx} < V_{DD/2} - 6x\ V_{DD}/20$

Drain-source monitoring threshold HB1-4

VDS1

Drain-source monitoring threshold HB1-4(0 0010$_B$)Reset Value:0000 0010 0100 1001$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HB4D	**HB3D**	**HB2D**	**HB1D**	**HB4VDSTH**			**HB3VDSTH**			**HB2VDSTH**			**HB1VDSTH**		
rw	rw	rw	rw	rw			rw			rw			rw		

Field	Bits	Type	Description
HB4D	15	rw	**HS4 Drain-source monitoring**[1)] 0_B Drain-source monitoring: DH - VSH4 (default) 1_B Drain-source monitoring: CSIN1 - VSH4
HB3D	14	rw	**HS3 Drain-source monitoring**[1)] 0_B Drain-source monitoring: DH - VSH3 (default) 1_B Drain-source monitoring: CSIN1 - VSH3
HB2D	13	rw	**HS2 Drain-source monitoring**[1)] 0_B Drain-source monitoring: DH - VSH2 (default) 1_B Drain-source monitoring: CSIN1 - VSH2
HB1D	12	rw	**HS1 Drain-source monitoring**[1)] 0_B Drain-source monitoring: DH - VSH1 (default) 1_B Drain-source monitoring: CSIN1 - VSH1
HB4VDSTH	11:9	rw	**HB4 drain-source overvoltage threshold** 000_B 0.15 V 001_B 0.20 V (default) 010_B 0.25 V 011_B 0.30 V 100_B 0.40 V 101_B 0.50 V 110_B 0.60 V 111_B 2.0 V
HB3VDSTH	8:6	rw	**HB3 drain-source overvoltage threshold** 000_B 0.15 V 001_B 0.20 V (default) 010_B 0.25 V 011_B 0.30 V 100_B 0.40V 101_B 0.50 V 110_B 0.60 V 111_B 2.0 V

Field	Bits	Type	Description
HB2VDSTH	5:3	rw	**HB2 drain-source overvoltage threshold** 000_B 0.15 V 001_B 0.20 V (default) 010_B 0.25 V 011_B 0.30 V 100_B 0.40 V 101_B 0.50 V 110_B 0.60 V 111_B 2.0 V
HB1VDSTH	2:0	rw	**HB1 drain-source overvoltage threshold** 000_B 0.15 V 001_B 0.20 V (default) 010_B 0.25 V 011_B 0.30 V 100_B 0.40 V 101_B 0.50 V 110_B 0.60 V 111_B 2.0 V

1) Applicable for HSx. The Drain-Source overvoltage for LSx is done by monitoring VSHx - VSL.

Cross current protection and blank time setting 1

CCP_BLK1
CCP and Blank times setting 1(0 0100_B)Reset Value: 0000 0000 0000 0000_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		**Reserved**		**Reserved**		**Reserved**		**HB4CCPBLK**		**HB3CCPBLK**		**HB2CCPBLK**		**HB1CCPBLK**	
r		r		r		r		rw		rw		rw		rw	

Field	Bits	Type	Description
Reserved	15:14	r	**Reserved. Always read as '0'**
Reserved	13:12	r	**Reserved. Always read as '0'**
Reserved	11:10	r	**Reserved. Always read as '0'**
Reserved	9:8	r	**Reserved. Always read as '0'**
HB4CCPBLK	7:6	rw	**Cross-current protection and blank times applied to HB4** 00_B (tHB4CCP, tHB4BLANK) = (tCCP1, tBLANK1) (default) 01_B (tHB4CCP, tHB4BLANK) = (tCCP2, tBLANK2) 10_B (tHB4CCP, tHB4BLANK) = (tCCP3, tBLANK3) 11_B (tHB4CCP, tHB4BLANK) = (tCCP4, tBLANK4)
HB3CCPBLK	5:4	rw	**Cross-current protection and blank times applied to HB3** 00_B (tHB3CCP, tHB3BLANK) = (tCCP1, tBLANK1) (default) 01_B (tHB3CCP, tHB3BLANK) = (tCCP2, tBLANK2) 10_B (tHB3CCP, tHB3BLANK) = (tCCP3, tBLANK3) 11_B (tHB3CCP, tHB3BLANK) = (tCCP4, tBLANK4)
HB2CCPBLK	3:2	rw	**Cross-current protection and blank times applied to HB2** 00_B (tHB2CCP, tHB2BLANK) = (tCCP1, tBLANK1) (default) 01_B (tHB2CCP, tHB2BLANK) = (tCCP2, tBLANK2) 10_B (tHB2CCP, tHB2BLANK) = (tCCP3, tBLANK3) 11_B (tHB2CCP, tHB2BLANK) = (tCCP4, tBLANK4)
HB1CCPBLK	1:0	rw	**Cross-current protection and blank times applied to HB1** 00_B (tHB1CCP, tHB1BLANK) = (tCCP1, tBLANK1) (default) 01_B (tHB1CCP, tHB1BLANK) = (tCCP2, tBLANK2) 10_B (tHB1CCP, tHB1BLANK) = (tCCP3, tBLANK3) 11_B (tHB1CCP, tHB1BLANK) = (tCCP4, tBLANK4)

Refer to **CCP_BLK2_ACT**, **PWM_ICHGMAX_CCP_BLK3_ACT**, **CCP_BLK2_FW** and **PWM_ICHGMAX_CCP_BLK3_FW** for the setting of (tCCPx, tBLANKx), x = 1 … 4.

Cross current protection and blank time setting 2 for active MOSFETs

Attention: ***This register is accessed with REG_BANK = 0 and the offset adress 0 0101$_B$. tCCP and tBLANK are applicable to the active MOSFETs.***

CCP_BLK2_ACT

Active CCP and Blank times setting 2(0 0101$_B$)Reset Value: 0100 1001 0010 0100$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TCCP3_ACT			TBLANK2_ACT			TCCP2_ACT			TBLANK1_ACT			TCCP1_ACT		
r	rw			rw			rw			rw			rw		

Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
TCCP3_ACT	14:12	rw	**Cross-current protection - tCCP3 Active** Refer to **Table 29** Default: 100$_B$: typ. 2000 ns
TBLANK2_ACT	11:9	rw	**Blank time - tBLANK2 Active** Refer to **Table 30** Default: 100$_B$: typ. 2000 ns
TCCP2_ACT	8:6	rw	**Cross-current protection - tCCP2 Active** Refer to **Table 29** Default: 100$_B$: typ. 2000 ns
TBLANK1_ACT	5:3	rw	**Blank time - tBLANK1 Active** Refer to **Table 30** Default: 100$_B$: typ. 2000 ns
TCCP1_ACT	2:0	rw	**Cross-current protection - tCCP1 Active** Refer to **Table 29** Default: 100$_B$: typ. 2000 ns

Table 29 Cross-current protection time for active MOSFETs

TCCPx_ACT[2:0], x = 1…4	Active cross-current protection HBx, x = 1…4 (typical)
000$_B$	375 ns
001$_B$	625 ns
010	1 µs
011	1.5 µs
100	2 µs (default)
101	3 µs
110	4 µs
111	16 µs[1)]

1) When applying a cross-current protection time of 16 µs to a half-bridge, the max. drive current used for this half-bridge must be set below 30 mA , to avoid an overheating of the gate driver. Refer to register **ST_ICHG** for static controlled half-bridges and **PWM_IDCHG_ACT** for half-bridges controlled in PWM.

Table 30 Drain-Source overvoltage blank time for active MOSFETs

TBLANKx_ACT[2:0], x = 1…4	Active drain-Source overvoltage blank time tBLANKx, x = 1…4 (typical)
000_B	625 ns
001_B	1 µs
010_B	1.25 µs
011_B	1.5 µs
100_B	2 µs (default)
101_B	3 µs
110_B	4 µs
111_B	16 µs[1)]

1) When applying a drain-source overvoltage blank time of 16 µs to a half-bridge, the max. drive current used for this half-bridge must be set below 30 mA , to avoid an overheating of the gate driver. Refer to register **ST_ICHG** for static controlled half-bridges and **PWM_ICHG_ACT** for half-bridges controlled in PWM.

Refer to **PWM_ICHGMAX_CCP_BLK3_ACT** for the setting of tBLANK4, tCCP4 and tBLANK3 for the active MOSFETs.

Refer to **CCP_BLK1** for the mapping of (tCCPx,tBLANKx) to the half-bridges.

Cross current protection and blank time setting 2 for FW MOSFETs

Attention: ***This register is accessed with REG_BANK = 1 and the offset address 0 0101$_B$. tCCP and tBLANK are applicable to the FW MOSFETs.***

CCP_BLK2_FW
FW CCP and Blank times setting 2(0 0101$_B$)Reset Value: 0100 1001 0010 0100$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TCCP3_FW			TBLANK2_FW			TCCP2_FW			TBLANK1_FW			TCCP1_FW		
r	rw			rw			rw			rw			rw		

Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
TCCP3_FW	14:12	rw	**Cross-current protection - tCCP3 Freewheeling** Refer to **Table 31** Default: 100$_B$: typ. 2000 ns
TBLANK2_FW	11:9	rw	**Blank time - tBLANK2 Freewheeling** Refer to **Table 32** Default: 100$_B$: typ. 2000 ns
TCCP2_FW	8:6	rw	**Cross-current protection - tCCP2 Freewheeling** Refer to **Table 31** Default: 100$_B$: typ. 2000 ns
TBLANK1_FW	5:3	rw	**Blank time - tBLANK1 Freewheeling** Refer to **Table 32** Default: 100$_B$: typ. 2000 ns
TCCP1_FW	2:0	rw	**Cross-current protection - tCCP1 Freewheeling** Refer to **Table 31** Default: 100$_B$: typ. 2000 ns

Table 31 Cross-current protection time for FW MOSFETs

TCCPx_FW[2:0], x = 1…4	FW cross-current protection HBx, x = 1…4 (typical)
000$_B$	375 ns
001$_B$	625 ns
010	1 µs
011	1.5 µs
100	2 µs (default)
101	3 µs
110	4 µs
111	16 µs[1)]

1) When applying a cross-current protection time of 16 µs to a half-bridge, the max. drive current used for this half-bridge must be set below 30 mA , to avoid an overheating of the gate driver. Refer to register **ST_ICHG** for static controlled half-bridges and **PWM_ICHG_FW** for half-bridges controlled in PWM.

Table 32 Drain-Source overvoltage blank time for FW MOSFETs

TBLANKx_FW[2:0], x = 1…4	FW Drain-Source overvoltage blank time tBLANKx, x = 1…4 (typical)
000_B	625 ns
001_B	1 µs
010_B	1.25 µs
011_B	1.5 µs
100_B	2 µs (default)
101_B	3 µs
110_B	4 µs
111_B	16 µs[1)]

1) When applying a drain-source overvoltage blank time of 16 µs to a half-bridge, the max. drive current used for this half-bridge must be set below 30 mA , to avoid an overheating of the gate driver. Refer to register **ST_ICHG** for static controlled half-bridges and **PWM_ICHG_FW** for half-bridges controlled in PWM.

Refer to **PWM_ICHGMAX_CCP_BLK3_FW** for the setting of tBLANK4, tCCP4 and tBLANK3 for the FW MOSFETs.

Refer to **CCP_BLK1** for the mapping of (tCCPx,tBLANKx) to the half-bridges.

9.1.2 Half-bridge control

Half-bridge mode

HBMODE
Half-bridge mode **(0 0110$_B$)Reset Value: 0$_B$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		Reserved		Reserved		Reserved		HB4MODE		HB3MODE		HB2MODE		HB1MODE	
r		r		r		r		rw		rw		rw		rw	

Field	Bits	Type	Description
Reserved	15:14	r	**Reserved. Always read as '0'**
Reserved	13:12	r	**Reserved. Always read as '0'**
Reserved	11:10	r	**Reserved. Always read as '0'**
Reserved	9:8	r	**Reserved. Always read as '0'**
HB4MODE	7:6	rw	**Half-bridge output 4 mode selection** 00_B HB4 is in high impedance (default) 01_B LS4 is ON 10_B HS4 is ON 11_B Reserved - HB4 is in high impedance
HB3MODE	5:4	rw	**Half-bridge output 3 mode selection** 00_B HB3 is in high impedance (default) 01_B LS3 is ON 10_B HS3 is ON 11_B Reserved - HB3 is in high impedance
HB2MODE	3:2	rw	**Half-bridge output 2 mode selection** 00_B HB2 is in high impedance (default) 01_B LS2 is ON 10_B HS2 is ON 11_B Reserved - HB2 is in high impedance
HB1MODE	1:0	rw	**Half-bridge output 1 mode selection** 00_B HB1 is in high impedance (default) 01_B LS1 is ON 10_B HS1 is ON 11_B Reserved - HB1 is in high impedance

PWM channel settings

Attention: This register is accessed only if REG_BANK = 0 with the corresponding offset address.

PWMSET
PWM channel settings (0 0111$_B$)Reset Value: 0110 0100 0010 0000$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	**PASS_VDS**	**PASS_MOD**		**PWM3_HB**			**PWM3_EN**	**PWM2_HB**			**PWM2_EN**	**PWM1_HB**			**PWM1_EN**
r	rw	rw		rw			rw	rw			rw	rw			rw

Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
PASS_VDS	14	rw	**Drain-Source monitoring in bridge passive mode** 0_B DS monitoring in bridge passive mode disabled 1_B DS monitoring in bridge passive mode enabled (Default)
PASS_MOD	13:12	rw	**Settings for bridge driver passive mode** 00_B LS1-4 are always off *Note: Changing PASS_MOD from 00_B to any other value requires to clear **DSOV**[1] first before writing PASS_MOD,* 01_B LS1-4 are always on (static brake) 10_B LS1-4 are activated if passive VS OV is detected (overvoltage brake) (Default) 11_B LS1-4 are activated if passive VS OV is detected and PWM1 = High (overvoltage brake conditioned by PWM1)
PWM3_HB	11:9	rw	**Allocation of the PWM channel 3** 000_B HB1 001_B HB2 010_B HB3 (Default) 011_B HB4 100_B HB1 101_B HB2 110_B HB3 111_B HB4
PWM3_EN	8	rw	**PWM channel 3 enable** 0_B PWM3 is disabled (default) 1_B PWM3 is enabled
PWM2_HB	7:5	rw	**Allocation of the PWM channel 2** 000_B HB1 001_B HB2 (Default) 010_B HB3 011_B HB4 100_B HB1 101_B HB2 110_B HB3 111_B HB4

Field	Bits	Type	Description
PWM2_EN	4	rw	**PWM channel 2 enable** 0_B PWM2 is disabled (default) 1_B PWM2 is enabled
PWM1_HB	3:1	rw	**Allocation of the PWM channel 1** 000_B HB1 (default) 001_B HB2 010_B HB3 011_B HB4 100_B HB1 101_B HB2 110_B HB3 111_B HB4
PWM1_EN	0	rw	**PWM channel 1 enable** 0_B PWM1 is disabled (default) 1_B PWM1 is enabled

1) If **DSOV** is not cleared first, the value of **PASS_MOD** stays at 00_B

If the same half-bridge is mapped to several activated PWM channels, then a SPI error is reported and the impacted half-bridge is in high-impedance.

PWM pre-charge and pre-discharge time

TPRECHG
Charge and pre-charge time **(0 1000_B) Reset Value: 0_B**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	EN_DEEP_AD	Reserved	EN_GEN_CHECK	TPDCHG3		TPCHG3		TPDCHG2		TPCHG2		TPDCHG1		TPCHG1	
rw	rw	rw	rw	rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
Reserved	15	rw	**Reserved. To be programmed as '0'.**
EN_DEEP_AD	14	rw	**Deep adaptation enabled** 0_B Deep adaptation disabled (default) 1_B Deep adaptation enabled. Refer to **Chapter 6.3.3.6**.
Reserved	13	rw	**Reserved. This bits must be set to '0'**
EN_GEN_CHECK	12	rw	**Enable generator check** 0_B Detection of generator mode disabled (default) 1_B Detection of generator mode enabled.
TPDCHG3	11:10	rw	**Pre-discharge time of PWM channel 3** 00_B 125 ns (default) 01_B 250 ns 10_B 500 ns 11_B 1000 ns
TPCHG3	9:8	rw	**Pre-charge time of PWM channel 3** 00_B 125 ns (default) 01_B 250 ns 10_B 500 ns 11_B 1000 ns
TPDCHG2	7:6	rw	**Pre-discharge time of PWM channel 2** 00_B 125 ns (default) 01_B 250 ns 10_B 500 ns 11_B 1000 ns
TPCHG2	5:4	rw	**Pre-charge time of PWM channel 2** 00_B 125 ns (default) 01_B 250 ns 10_B 500 ns 11_B 1000 ns
TPDCHG1	3:2	rw	**Pre-discharge time of PWM channel 1** 00_B 125 ns (default) 01_B 250 ns 10_B 500 ns 11_B 1000 ns

Field	Bits	Type	Description
TPCHG1	1:0	rw	**Pre-charge time of PWM channel 1** 00_B 125 ns (default) 01_B 250 ns 10_B 500 ns 11_B 1000 ns

Half-bridge diagnostic current control

HBIDIAG
Half-bridge diagnostic current control(0 1001_B)Reset Value: 1100 0000 0000 0000_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSA2L	CSA1L	OC2FILT		OC1FILT		CSA2_OFF	CSA1_OFF	Reserved	Reserved	Reserved	Reserved	HB4IDIAG	HB3IDIAG	HB2IDIAG	HB1IDIAG
rw	rw	rw		rw		rw	rw	r	r	r	r	rw	rw	rw	rw

Field	Bits	Type	Description
CSA2L	15	rw	**Level of CSA2** 0_B CSA2 is configured as low-side 1_B CSA2 is configured as high-side (default)
CSA1L	14	rw	**Level of CSA1** 0_B CSA1 is configured as low-side 1_B CSA1 is configured as high-side (default)
OC2FILT	13:12	rw	**Overcurrent filter time for CSO2** 00_B 6 µs (default) 01_B 10 µs 10_B 50 µs 11_B 100 µs
OC1FILT	11:10	rw	**Overcurrent filter time for CSO1** 00_B 6 µs (default) 01_B 10 µs 10_B 50 µs 11_B 100 µs
CSA2_OFF	9	rw	**Disable of CSA2** 0_B CSA2 enabled(default) 1_B CSA2 disabled
CSA1_OFF	8	rw	**Disable of CSA1** 0_B CSA1 enabled (default) 1_B CSA1 disabled
Reserved	7	r	**Reserved. Always read as ‘0’**
Reserved	6	r	**Reserved. Always read as ‘0’**
Reserved	5	r	**Reserved. Always read as ‘0’**
Reserved	4	r	**Reserved. Always read as ‘0’**
HB4IDIAG	3	rw	**Control of HB4 off-state current source and current sink** 0_B Pull-down deactivated (default) 1_B Pull-down activated
HB3IDIAG	2	rw	**Control of HB3 off-state current source and current sink** 0_B Pull-down deactivated (default) 1_B Pull-down activated
HB2IDIAG	1	rw	**Control of HB2 off-state current source and current sink** 0_B Pull-down deactivated (default) 1_B Pull-down activated

Field	Bits	Type	Description
HB1IDIAG	0	rw	**Control of HB1 pull-down for off-state diagnostic** 0_B Pull-down deactivated (default) 1_B Pull-down activated

Static charge and discharge current selection

Attention: This register is accessed only if REG_BANK = 0 with the corresponding offset address.

ST_ICHG
Static charge and discharge current selection(0 1010$_B$)Reset Value: 0000 0000 0100 0100$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	HB4ICHGST	HB3ICHGST	HB2ICHGST	HB1ICHGST	ICHGST2				ICHGST1			
r	r	r	r	rw	rw	rw	rw	rw				rw			

Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
Reserved	14	r	**Reserved. Always read as '0'**
Reserved	13	r	**Reserved. Always read as '0'**
Reserved	12	r	**Reserved. Always read as '0'**
HB4ICHGST	11	rw	**HB4 Selection of charge and discharge currents** 0_B The static charge/discharge current 1 is applied to the half-bridge 4 (default). 1_B The static charge/discharge current 2 is applied to the half-bridge 4.
HB3ICHGST	10	rw	**HB3 Selection of charge and discharge currents** 0_B The static charge/discharge current 1 is applied to the half-bridge 3 (default). 1_B The static charge/discharge current 2 is applied to the half-bridge 3.
HB2ICHGST	9	rw	**HB2 Selection of charge and discharge currents** 0_B The static charge/discharge current 1 is applied to the half-bridge 2 (default). 1_B The static charge/discharge current 2 is applied to the half-bridge 2.
HB1ICHGST	8	rw	**HB1 Selection of charge and discharge currents** 0_B The static charge/discharge current 1 is applied to the half-bridge 1 (default). 1_B The static charge/discharge current 2 is applied to the half-bridge 1.
ICHGST2	7:4	rw	**Static gate driver charge and discharge currents 2** Refer to **Table 10** Default: 0100_B - Charge 12.5 mA typ., discharge 14.2 mA typ.
ICHGST1	3:0	rw	**Static gate driver charge and discharge currents 1** Refer to **Table 10** Default: 0100_B - charge 12.5 mA typ., discharge 14.2 mA typ.

PWM Active MOSFET precharge current initialization

Attention: ***This register is accessed only if REG_BANK = 1 with the corresponding offset address.***

PWM_PCHG_INIT
Initial PWM precharge current selection(0 1010_B)Reset Value: 0001 1000 1100 0110_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	PCHGINIT3					PCHGINIT2					PCHGINIT1				
r	rw					rw					rw				

Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
PCHGINIT3	14:10	rw	**Initial precharge current of PWM Channel 3** Refer to **Table 13** Default: 00110_B: typ. 8.0 mA
PCHGINIT2	9:5	rw	**Initial precharge current of PWM Channel 2** Refer to **Table 13** Default: 00110_B: typ. 8.0 mA
PCHGINIT1	4:0	rw	**Initial precharge current of PWM Channel 1** Refer to **Table 13** Default: 00110_B: typ. 8.0 mA

PWM charge current of active MOSFETs

Attention: ***This register is accessed with REG_BANK = 0 and the offset address 0 1011$_B$. The charge currents are applied to the active MOSFET (ICHG1-3).***

PWM_ICHG_ACT
Active PWM charge current (0 1011$_B$)Reset Value:0001 1000 1100 0110$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	ICHG3					ICHG2					ICHG1				
r	rw					rw					rw				

Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
ICHG3	14:10	rw	**Gate driver charge current of PWM Channel 3 (Active MOSFET)** Refer to **Table 13** Default: 00110$_B$: typ. 8.0 mA
ICHG2	9:5	rw	**Gate driver charge current of PWM Channel 2 (Active MOSFET)** Refer to **Table 13** Default: 00110$_B$: typ. 8.0 mA
ICHG1	4:0	rw	**Gate driver charge current of PWM Channel 1 (Active MOSFET)** Refer to **Table 13** Default: 00110$_B$: typ. 8.0 mA

PWM charge/discharge currents of FW MOSFETs

Attention: ***This register is accessed with REG_BANK = 1 and the offset address 0 1011$_B$. The charge and discharge currents are applied to the freewheeling MOSFETs (ICHGFW1-3).***

PWM_ICHG_FW

FW PWM charge/discharge currents (0 1011$_B$) Reset Value:0001 1000 1100 0110$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	ICHG3_FW					ICHG2_FW					ICHG1_FW				
r	rw					rw					rw				

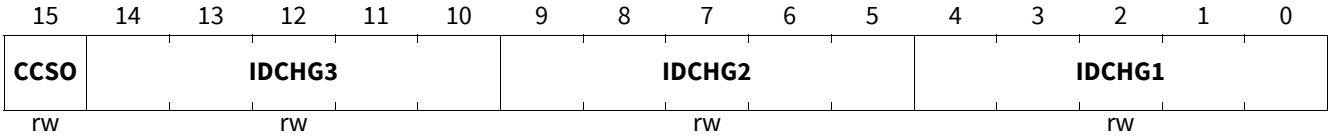
Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
ICHG3_FW	14:10	rw	**Gate driver charge and discharge currents of PWM Channel 3 (FW MOSFET)** Refer to **Table 13**, **Table 14** Default: 00110$_B$. Typ. charge 8.0 mA, typ. discharge: 9.4 mA
ICHG2_FW	9:5	rw	**Gate driver charge and discharge currents of PWM Channel 2 (FW MOSFET)** Refer to **Table 13**, **Table 14** Default: 00110$_B$. Typ. charge 8.0 mA, typ. discharge: 9.4 mA
ICHG1_FW	4:0	rw	**Gate driver charge and discharge currents of PWM Channel 1 (FW MOSFET)** Refer to **Table 13**, **Table 14** Default: 00110$_B$. Typ. charge 8.0 mA, typ. discharge: 9.4 mA

Note: The selected currents are applied to the turn-on and the turn-off of the FW MOSFETs.

PWM discharge current for active MOSFETs

Attention: This register is accessed only if REG_BANK = 0 with the corresponding offset address.

PWM_IDCHG_ACT
PWM discharge current (0 1100$_B$)Reset Value: 0001 1100 1110 0111$_B$



Field	Bits	Type	Description
CCSO	15	rw	**Capacitor connected to the current sense amplifier outputs** 0_B Capacitor connected to CSO < 100 pF (default) 1_B Capacitor connected to CSO < 400 pF
IDCHG3	14:10	rw	**Discharge current for PWM Channel 3 (Active MOSFET)** Refer to **Table 14** Default: 00111_B: typ. 11.8 mA
IDCHG2	9:5	rw	**Discharge current for PWM Channel 2 (Active MOSFET)** Refer to **Table 14** Default: 00111_B: typ. 11.8 mA
IDCHG1	4:0	rw	**Discharge current of PWM Channel 1 (Active MOSFET)** Refer to **Table 14** Default: 00111_B: typ. 11.8 mA

PWM Active MOSFET predischarge current initialization

Attention: This register is accessed only if REG_BANK = 1 with the corresponding offset address.

PWM_PDCHG_INIT
Initial PWM predischarge current selection(0 1100_B)Reset Value: 0011 0001 1000 1100_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCSO	PDCHGINIT3					PDCHGINIT2					PDCHGINIT1				
rw	rw					rw					rw				

Field	Bits	Type	Description
CCSO	15	rw	**Capacitor connected to the current sense amplifier outputs** 0_B Capacitor connected to CSO < 100 pF (default) 1_B Capacitor connected to CSO < 400 pF
PDCHGINIT3	14:10	rw	**Initial predischarge current of PWM Channel 3** Refer to **Table 14** Default: 01100_B: typ. 26.0 mA
PDCHGINIT2	9:5	rw	**Initial predischarge current of PWM Channel 2** Refer to **Table 14** Default: 01100_B: typ. 26.0 mA
PDCHGINIT1	4:0	rw	**Initial predischarge current of PWM Channel 1** Refer to **Table 14** Default: 01100_B: typ. 26.0 mA

PWM maximum drive current selection and active tCCP4, tBLANK 3/4

Attention: ***This register is accessed with REG_BANK = 0 and the offset address 0 1101$_B$. tCCP and tBLANK are applicable to the active MOSFETs.***

PWM_ICHGMAX_CCP_BLK3_ACT

PWM max. drive current (0 1101$_B$)Reset Value: 0100 1001 0000 0000$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TBLANK4_ACT			TCCP4_ACT			TBLANK3_ACT			ICHGMAX3		ICHGMAX2		ICHGMAX1	
r	rw			rw			rw			rw		rw		rw	

Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
TBLANK4_ACT	14:12	rw	**Blank time [1] - tBLANK4 Active** Refer to **Table 30** Default: 100$_B$: typ. 2000 ns
TCCP4_ACT	11:9	rw	**Cross-current protection[1] - tCCP4 Active** Refer to **Table 29** Default: 100$_B$: typ. 2000 ns
TBLANK3_ACT	8:6	rw	**Blank time[1] - tBLANK3 Active** Refer to **Table 30** Default: 100$_B$: typ. 2000 ns
ICHGMAX3	5:4	rw	**Maximum drive current of half-bridge mapped to PWM channel 3 during the pre-charge phase and pre-discharge phases[2]** 00$_B$ (default) charge: typ. 18.8 mA, discharge: typ. 19.7 mA 01$_B$ charge: typ. 41mA, discharge: typ. 43 mA 10$_B$ charge: typ. 77 mA, discharge: typ. 79 mA 11$_B$ charge: typ. 100 mA, discharge: typ. 100 mA
ICHGMAX2	3:2	rw	**Maximum drive current of half-bridge mapped to PWM channel 2 during the pre-charge phase and pre-discharge phases[2]** 00$_B$ (default) charge: typ. 18.8 mA, discharge: typ. 19.7 mA 01$_B$ charge: typ. 41 mA, discharge: typ. 43 mA 10$_B$ charge: typ. 77 mA, discharge: typ. 79 mA 11$_B$ charge: typ. 100 mA, discharge: typ. 100 mA
ICHGMAX1	1:0	rw	**Maximum drive current of half-bridge mapped to PWM channel 1 during the pre-charge and pre-discharge phases[2]** 00$_B$ (default) charge: typ. 18.8 mA, discharge: typ. 19.7 mA 01$_B$ charge: typ. 41 mA, discharge: typ. 43 mA 10$_B$ charge: typ. 77 mA, discharge: typ. 79 mA 11$_B$ charge: typ. 100 mA, discharge: typ. 100 mA

1) Refer to **CCP_BLK1** for the mapping of (tCCPx,tBLANKx) to the half-bridges.

2) ICHGMAX is also the current applied during the post-charge of the PWM MOSFET Refer to **Table 12**.

PWM maximum drive current selection and FW tCCP4, tBLANK 3/4

Attention: ***This register is accessed with REG_BANK = 1 and the offset address 0 1101$_B$. tCCP and tBLANK are applicable to the FW MOSFETs.***

PWM_ICHGMAX_CCP_BLK3_FW

PWM max. drive current (0 1101$_B$)Reset Value: 0100 1001 0000 0000$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TBLANK4_FW			TCCP4_FW			TBLANK3_FW			ICHGMAX3		ICHGMAX2		ICHGMAX1	
r	rw			rw			rw			rw		rw		rw	

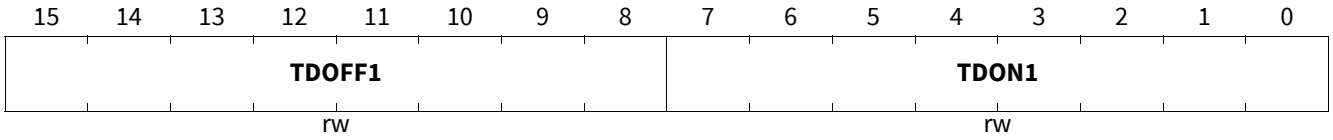
Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
TBLANK4_FW	14:12	rw	**Blank time [1] - tBLANK4 Freewheeling** Refer to **Table 32** Default: 100$_B$: typ. 2000 ns
TCCP4_FW	11:9	rw	**Cross-current protection[1] - tCCP4 Freewheeling** Refer to **Table 31** Default: 100$_B$: typ. 2000 ns
TBLANK3_FW	8:6	rw	**Blank time[1] - tBLANK3 Freewheeling** Refer to **Table 32** Default: 100$_B$: typ. 2000 ns
ICHGMAX3	5:4	rw	**Maximum drive current of half-bridge mapped to PWM channel 3 during the pre-charge phase and pre-discharge phases[2]** 00$_B$ (default) charge: typ. 19 mA, discharge: typ. 19 mA 01$_B$ charge: typ. 41mA, discharge: typ. 43 mA 10$_B$ charge: typ. 77 mA, discharge: typ. 79 mA 11$_B$ charge: typ. 100 mA, discharge: typ. 100 mA
ICHGMAX2	3:2	rw	**Maximum drive current of half-bridge mapped to PWM channel 2 during the pre-charge phase and pre-discharge phases[2]** 00$_B$ (default) charge: typ. 19 mA, discharge: typ. 19 mA 01$_B$ charge: typ. 41mA, discharge: typ. 43 mA 10$_B$ charge: typ. 77 mA, discharge: typ. 79 mA 11$_B$ charge: typ. 100 mA, discharge: typ. 100 mA
ICHGMAX1	1:0	rw	**Maximum drive current of half-bridge mapped to PWM channel 1 during the pre-charge and pre-discharge phases[2]** 00$_B$ (default) charge: typ. 19 mA, discharge: typ. 19 mA 01$_B$ charge: typ. 41mA, discharge: typ. 43 mA 10$_B$ charge: typ. 77 mA, discharge: typ. 79 mA 11$_B$ charge: typ. 100 mA, discharge: typ. 100 mA

1) Refer to **CCP_BLK1** for the mapping of (tCCPx,tBLANKx) to the half-bridges.

2) ICHGMAX is also the current applied during the post-charge of the PWM MOSFET Refer to **Table 12**.

Selection MOSFET turn-on and turn-off delay for PWM channel 1

TDON_OFF1
MOSFET turn-on/off delay of PWM channel1 (0 1110_B)Reset Value:0000 1010 0000 1010_B



Field	Bits	Type	Description
TDOFF1	15:8	rw	**Turn-off delay time of PWM Channel 1.** Typical TDOFF1 = 62.5 x $TDOFF1[7:0]_D$ ns Default: 0000 1010_B: 625 ns typ.
TDON1	7:0	rw	**Turn-on delay time of PWM Channel 1.** Typical TDON1 = 62.5 x $TDON1[7:0]_D$ ns Default: 0000 1010_B: 625 ns typ.

Selection MOSFET turn-on and turn-off delay for PWM channel 2

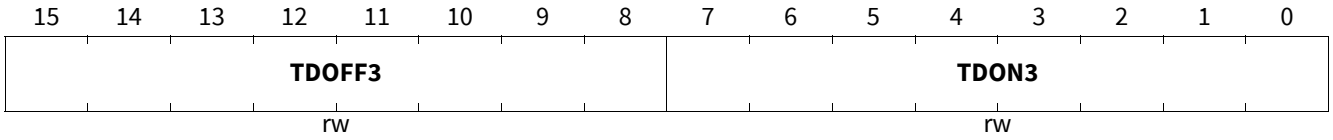
TDON_OFF2
MOSFET turn-on/off delay of PWM channel2 (0 1111_B)Reset Value: 0000 1010 0000 1010_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDOFF2								**TDON2**							
rw								rw							

Field	Bits	Type	Description
TDOFF2	15:8	rw	**Turn-off delay time of PWM Channel 2.** Typical TDOFF2 = 62.5 x $TDOFF2[7:0]_D$ ns Default: 0000 1010_B: 625 ns typ.
TDON2	7:0	rw	**Turn-on delay time of PWM Channel 2.** Typical TDON2 = 62.5 x $TDON2[7:0]_D$ ns Default: 0000 1010_B: 625 ns typ.

Selection MOSFET turn-on and turn-off delay for PWM channel 3

TDON_OFF3
MOSFET turn-on/off delay of PWM channel3 (1 0000_B)Reset Value: 0000 1010 0000 1010_B



Field	Bits	Type	Description
TDOFF3	15:8	rw	**Turn-off delay time of PWM Channel 3.** Typical TDOFF3 = 62.5 x $TDOFF3[7:0]_D$ ns Default: $0000\ 1010_B$: 625 ns typ.
TDON3	7:0	rw	**Turn-on delay time of PWM Channel 3.** Typical TDON3 = 62.5 x $TDON3[7:0]_D$ ns Default: $0000\ 1010_B$: 625 ns typ.

9.2 Status register

Table 33 Register Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
GENSTAT	General status register	11_H	0_H
DSOV	Drain-source overvoltage	12_H	0_H
HBVOUT_PWMERR	Half-Bridge output voltage	13_H	0_H
EFF_TDON_OFF1	Effective MOSFET turn-on and turn-off delays for PWM Channel 1	14_H	0_H
EFF_TDON_OFF2	Effective MOSFET turn-on and turn-off delays for PWM Channel 2	15_H	0_H
EFF_TDON_OFF3	Effective MOSFET turn-on and turn-off delays for PWM Channel 3	16_H	0_H
TRISE_FALL1	Effective MOSFET rise and fall times for PWM Channel 1	17_H	0_H
TRISE_FALL2	Effective MOSFET rise and fall times for PWM Channel 2	18_H	0_H
TRISE_FALL3	Effective MOSFET rise and fall times for PWM Channel 3	19_H	0_H
DEVID	Device identifier	$1F_H$	81_H

9.2.1 General status register

General status register

GENSTAT
General Status Register **(1 0001$_B$)Reset Value: 0$_B$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PASS_VDSOV	WDMON		PWM3STAT	PWM2STAT	PWM1STAT	TDREG3	TDREG2	TDREG1	TSD	TW	OC2	OC1	VSOV	VSUV	CPUV
r	r		r	r	r	rc	rc	rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
PASS_VDSOV	15	r	**DS overvoltage while the bridge driver is in passive mode** 0$_B$ No overvoltage on drain-source of any low-sides (default) 1$_B$ Overvoltage on drain-source of one of the low-side is detected.
WDMON	14:13	r	**Watchdog Monitoring** 00$_B$ WD Timer is between [0%;25%[of the WD period (default) 01$_B$ WD Timer is between [25%;50%[of the WD period 10$_B$ WD Timer is between [50%;75%[of the WD period 11$_B$ WD Timer is between [75%;100 %[of the WD period
PWM3STAT	12	r	**Status of PWM3 input** 0$_B$ PWM3 is low (default) 1$_B$ PWM3 is high
PWM2STAT	11	r	**Status of PWM2 input** 0$_B$ PWM2 is low (default) 1$_B$ PWM2 is high
PWM1STAT	10	r	**Status of PWM1 input** 0$_B$ PWM1 is low (default) 1$_B$ PWM1 is high
TDREG3	9	rc	**PWM channel 3 - Regulation of turn-on and turn-off delays** 0$_B$ the turn-on delay or the turn-off delay are not in regulation (default) 1$_B$ the turn-on and turn-off delays are in regulation
TDREG2	8	rc	**PWM channel 2 - Regulation of turn-on and turn-off delays** 0$_B$ the turn-on delay or the turn-off delay are not in regulation (default) 1$_B$ the turn-on and turn-off delays are in regulation
TDREG1	7	rc	**PWM channel 1 - Regulation of turn-on and turn-off delays** 0$_B$ the turn-on delay or the turn-off delay are not in regulation (default) 1$_B$ the turn-on and turn-off delays are in regulation
TSD	6	rc	**Thermal Shutdown** 0$_B$ No thermal shutdown is detected (default) 1$_B$ A thermal shutdown is detected [2)]

Field	Bits	Type	Description
TW	5	rc	**Thermal Warning** 0_B No thermal warning is detected (default) 1_B A thermal warning is detected
OC2	4	rc	**Overcurrent detection of CSO2** 0_B No overcurrent detection on CSO2 (default) 1_B Overcurrent detected on CSO2[1)]
OC1	3	rc	**Overcurrent detection of CSO1** 0_B No overcurrent detection on CSO1 (default) 1_B Overcurrent detected on CSO1[1)]
VSOV	2	rc	**VS Overvoltage** 0_B No overvoltage on V_S detected (default value) 1_B Overvoltage on V_S detected[2)]
VSUV	1	rc	**VS Undervoltage** 0_B No undervoltage on V_S detected (default value) 1_B Undervoltage on V_S detected[2)]
CPUV	0	rc	**Charge Pump Undervoltage** 0_B No charge pump undervoltage (default) 1_B A charge pump undervoltage is detected[2)]

1) The state of the external MOSFETs depends on the setting of OCEN bit (see **GENCTRL1**).

2) The error is latched and the external MOSFETs are turned off.

Register specification

Drain-Source Overvoltage 1

DSOV
Drain-Source Overvoltage **($1\ 0010_B$)Reset Value: 0_B**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**LS4DSOV**	**HS4DSOV**	**LS3DSOV**	**HS3DSOV**	**LS2DSOV**	**HS2DSOV**	**LS1DSOV**	**HS1DSOV**
r	r	r	r	r	r	r	r	rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
Reserved	14	r	**Reserved. Always read as '0'**
Reserved	13	r	**Reserved. Always read as '0'**
Reserved	12	r	**Reserved. Always read as '0'**
Reserved	11	r	**Reserved. Always read as '0'**
Reserved	10	r	**Reserved. Always read as '0'**
Reserved	9	r	**Reserved. Always read as '0'**
Reserved	8	r	**Reserved. Always read as '0'**
LS4DSOV	7	rc	**Drain-Source overvoltage on low-side 4** 0_B No overvoltage on drain-source of low-side 4 (default) 1_B Overvoltage on drain-source of low-side 4 detected.
HS4DSOV	6	rc	**Drain-Source overvoltage on high-side 4** 0_B No overvoltage on drain-source of high-side 4 (default) 1_B Overvoltage on drain-source of high-side 4 detected.
LS3DSOV	5	rc	**Drain-Source overvoltage on low-side 3** 0_B No overvoltage on drain-source of low-side 3 (default) 1_B Overvoltage on drain-source of low-side 3 detected.
HS3DSOV	4	rc	**Drain-Source overvoltage on high-side 3** 0_B No overvoltage on drain-source of high-side 3 (default) 1_B Overvoltage on drain-source of high-side 3 detected.
LS2DSOV	3	rc	**Drain-Source overvoltage on low-side 2** 0_B No overvoltage on drain-source of low-side 2 (default) 1_B Overvoltage on drain-source of low-side 2 detected.
HS2DSOV	2	rc	**Drain-Source overvoltage on high-side 2** 0_B No overvoltage on drain-source of high-side 2 (default) 1_B Overvoltage on drain-source of high-side 2 detected.
LS1DSOV	1	rc	**Drain-Source overvoltage on low-side 1** 0_B No overvoltage on drain-source of low-side 1 (default) 1_B Overvoltage on drain-source of low-side 1 detected.
HS1DSOV	0	rc	**Drain-Source overvoltage on high-side 1** 0_B No overvoltage on drain-source of high-side 1 (default) 1_B Overvoltage on drain-source of high-side 1 detected.

Note: The impacted MOSFET is latched off if a Drain-Source overvoltage is detected.

Half-bridge Output Voltage Status

HBVOUT_PWMERR
Half-bridge output voltage and PWM Error(1 0011$_B$)Reset Value: 0$_B$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	HB4PWME	HB3PWME	HB2PWME	HB1PWME	Reserved	Reserved	Reserved	Reserved	HB4VOUT	HB3VOUT	HB2VOUT	HB1VOUT
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
Reserved	14	r	**Reserved. Always read as '0'**
Reserved	13	r	**Reserved. Always read as '0'**
Reserved	12	r	**Reserved. Always read as '0'**
HB4PWME	11	r	**PWM Error on HB4** 0_B No PWM error (default) 1_B More than one activated PWM channels is mapped to HB4[1)]
HB3PWME	10	r	**PWM Error on HB3** 0_B No PWM error (default) 1_B More than one activated PWM channels is mapped to HB3[1)]
HB2PWME	9	r	**PWM Error on HB2** 0_B No PWM error (default) 1_B More than one activated PWM channels is mapped to HB2[1)]
HB1PWME	8	r	**PWM Error on HB1** 0_B No PWM error (default) 1_B More than one activated PWM channels is mapped to HB1[1)]
Reserved	7	r	**Reserved**
Reserved	6	r	**Reserved**
Reserved	5	r	**Reserved**
Reserved	4	r	**Reserved**
HB4VOUT	3	r	**Voltage level at SH4 when HB4MODE[1:0] = (0,0) or (1,1):** 0_B Low: |VDH - VSH4| >$V_{VDSMONTHx}$ [2)]if HB4D = 0 |VCSIN1 - VSH4| >$V_{VDSMONTHx}$ if HB4D = 1 1_B High: |VDH - VSH4| <$V_{VDSMONTHx}$ if HB4D = 0; |VCSIN1 - VSH4| < $V_{VDSMONTHx}$ if HB4D = 1 *Note: HB4VOUT = 0 if HB4MODE[1:0]= (0,1) or (1,0)*
HB3VOUT	2	r	**Voltage level at SH3 when HB3MODE[1:0] = (0,0) or (1,1):** 0_B Low: |VDH - VSH3| >$V_{VDSMONTHx}$ [2)]if HB3D = 0 |VCSIN1 - VSH3| >$V_{VDSMONTHx}$ if HB3D = 1 1_B High: |VDH - VSH3| <$V_{VDSMONTHx}$ if HB3D = 0; |VCSIN1 - VSH3| < $V_{VDSMONTHx}$ if HB3D = 1 *Note: HB3VOUT = 0 if HB3MODE[1:0]= (0,1) or (1,0)*

Field	Bits	Type	Description
HB2VOUT	1	r	**Voltage level at SH2 when HB2MODE[1:0] = (0,0) or (1,1):** 0_B Low: |VDH - VSH2| >$V_{VDSMONTHx}$ [2] if HB2D = 0 |VCSIN1 - VSH2| >$V_{VDSMONTHx}$ if HB2D = 1 1_B High: |VDH - VSH2| <$V_{VDSMONTHx}$ if HB2D = 0; |VCSIN1 - VSH2| < $V_{VDSMONTHx}$ if HB2D = 1 *Note: HB2VOUT = 0 if HB2MODE[1:0]= (0,1) or (1,0)*
HB1VOUT	0	r	**Voltage level at SH1 when HB1MODE[1:0] = (0,0) or (1,1):** 0_B Low: |VDH - VSH1| >$V_{VDSMONTHx}$ [2] if HB1D = 0; |VCSIN1 - VSH1| >$V_{VDSMONTHx}$ if HB1D = 1 1_B High: |VDH - VSH1| <$V_{VDSMONTHx}$ if HB1D = 0; |VCSIN1 - VSH1| < $V_{VDSMONTHx}$ if HB1D = 1 *Note: HB1VOUT = 0 if HB1MODE[1:0]= (0,1) or (1,0)*

1) The bit is reset only if one PWM channel or no PWM channel is mapped to the half-bridge (refer to **PWMSET**).

2) $V_{VDSMONTHx}$ is the drain-source monitoring threshold selected for the corresponding half-bridge.

Effective MOSFET turn-on and turn-off delay of PWM1

EFF_TDON_OFF1
Effective MOSFET turn-on/off delay PWM1(1 0100_B)Reset Value: 0_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDOFF1EFF								**TDON1EFF**							
r								r							

Field	Bits	Type	Description
TDOFF1EFF	15:8	r	**Effective MOSFET turn-off delay of PWM Channel 1** Effective turn-off delay = 62.5 x $TDOFF1EFF[7:0]_D$ ns Default: 0_B
TDON1EFF	7:0	r	**Effective MOSFET turn-on delay of PWM Channel 1** Effective turn-on delay = 62.5 x $TDON1EFF[7:0]_D$ ns Default: 0_B

Effective MOSFET turn-on and turn-off delay of PWM2

EFF_TDON_OFF2
Effective MOSFET turn-on/off delay PWM2(1 0101_B)Reset Value: 0_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDOFF2EFF								TDON2EFF							
r								r							

Field	Bits	Type	Description
TDOFF2EFF	15:8	r	**Effective MOSFET turn-off delay of PWM Channel 2** Effective turn-off delay = 62.5 x TDOFF2EFF[7:0]$_D$ ns Default: 0_B
TDON2EFF	7:0	r	**Effective MOSFET turn-on delay of PWM Channel 2** Effective turn-on delay = 62.5 x TDON2EFF[7:0]$_D$ ns Default: 0_B

Effective MOSFET turn-on and turn-off delay of PWM3

EFF_TDON_OFF3
Effective MOSFET turn-on/off delay PWM3(1 0110_B)Reset Value: 0_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDOFF3EFF								**TDON3EFF**							
r								r							

Field	Bits	Type	Description
TDOFF3EFF	15:8	r	**Effective MOSFET turn-off delay of PWM Channel 3** Effective turn-off delay = 62.5 x TDOFF3EFF[7:0]$_D$ ns Default: 0_B
TDON3EFF	7:0	r	**Effective MOSFET turn-on delay of PWM Channel 3** Effective turn-on delay = 62.5 x TDON3EFF[7:0]$_D$ ns Default: 0_B

Effective MOSFET rise and fall times of PWM channel 1

TRISE_FALL1
Effective PWM MOSFET rise and fall times PWM1 (1 0111_B)Reset Value: 0_B

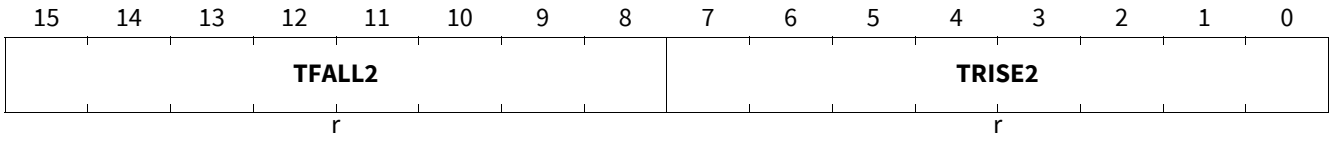
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFALL1								TRISE1							
r								r							

Field	Bits	Type	Description
TFALL1	15:8	r	**MOSFET fall time of PWM Channel 1** MOSFET fall time = 62.5 x TFALL1[7:0]$_D$ ns Default: 0_B
TRISE1	7:0	r	**MOSFET rise time of PWM Channel 1** MOSFET rise time = 62.5 x TRISE1[7:0]$_D$ ns Default: 0_B

Effective MOSFET rise and fall times of PWM channel 2

TRISE_FALL2

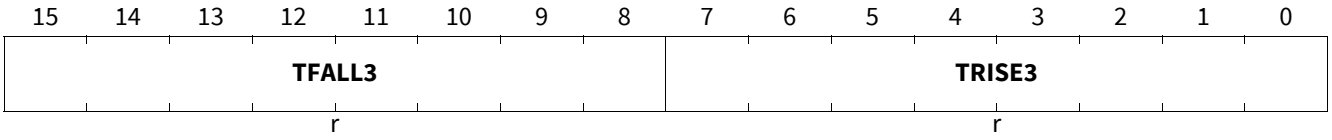
Effective PWM MOSFET rise and fall times PWM2 ($1\ 1000_B$)Reset Value: 0_B



Field	Bits	Type	Description
TFALL2	15:8	r	**MOSFET fall time of PWM Channel 2** MOSFET fall time = 62.5 x TFALL2[7:0]$_D$ ns Default: 0_B
TRISE2	7:0	r	**MOSFET rise time of PWM Channel 2** MOSFET rise time = 62.5 x TRISE2[7:0]$_D$ ns Default: 0_B

Effective MOSFET rise and fall times of PWM channel 3

TRISE_FALL3
Effective PWM MOSFET rise and fall times PWM3 (1 1001_B)Reset Value: 0_B



Field	Bits	Type	Description
TFALL3	15:8	r	**MOSFET fall time of PWM Channel 3** MOSFET fall time = 62.5 x TFALL3[7:0]$_D$ ns Default: 0_B
TRISE3	7:0	r	**MOSFET rise time of PWM Channel 3** MOSFET rise time = 62.5 x TRISE3[7:0]$_D$ ns Default: 0_B

Register specification

Device Identifier

DEVID
Device Identifier **(1 1111$_B$)Reset Value: 1000 0001$_B$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved							Reserved	Reserved		Reserved		DEV_ID		
r	r							r	r		r		r		

Field	Bits	Type	Description
Reserved	15	r	**Reserved. Always read as '0'**
Reserved	14:8	r	**Reserved. Always read as '0'**
Reserved	7	r	**Reserved. Always read as '1'**
Reserved	6:5	r	**Reserved.**
Reserved	4:3	r	**Reserved.**
DEV_ID	2:0	r	**Device derivative identifier** 000_B Reserved 001_B TLE92104-232 010_B Reserved 011_B Reserved 100_B Reserved 101_B Reserved 110_B Reserved 111_B TLE92104-131

10 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

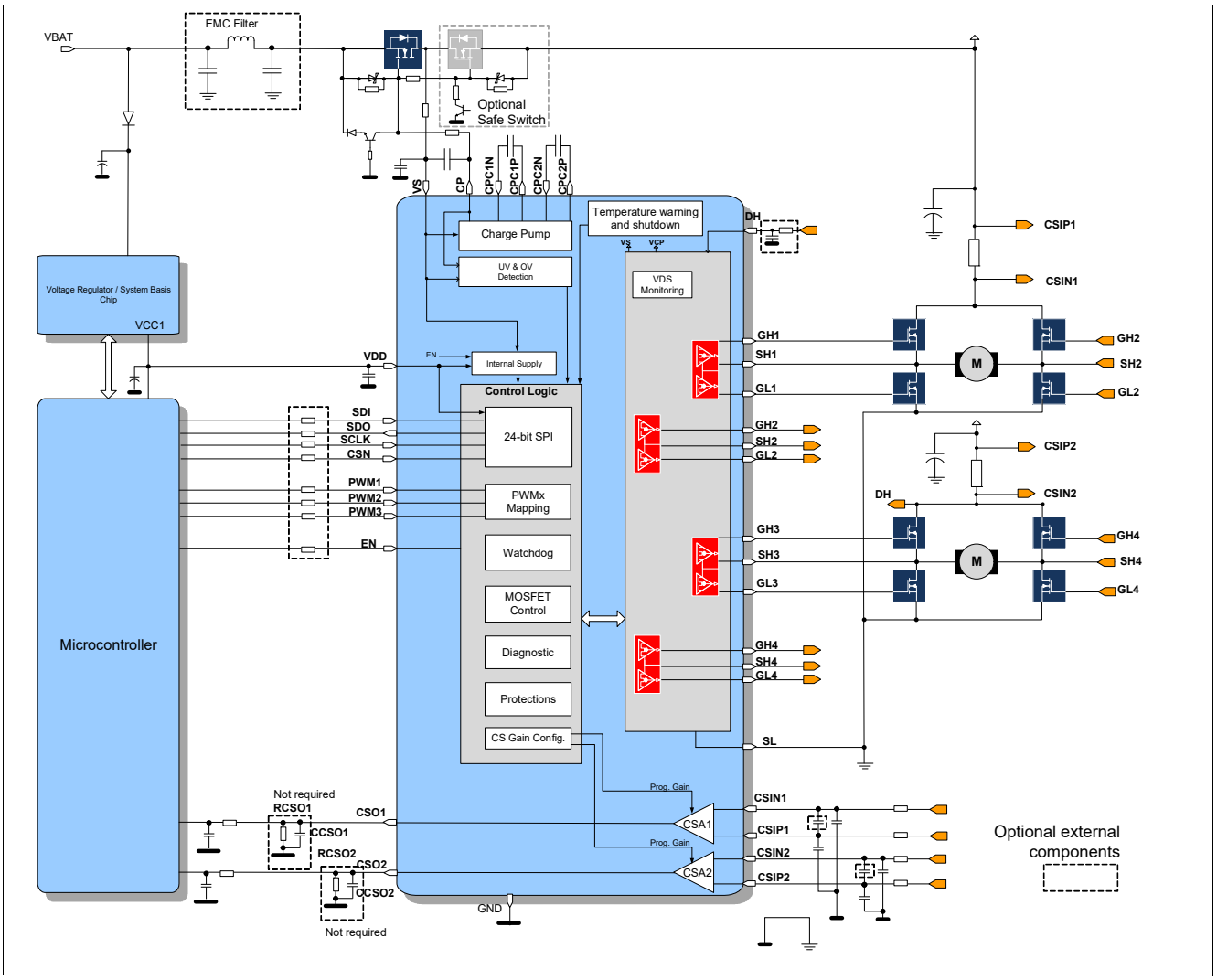


Figure 50 Application diagram TLE92104-232QX

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

The charge pump buffer capacitor between VS and CP must have a capacitance equal or higher than 470 nF for a stable operation. A higher capacitance can be used to reduce the voltage ripples caused by the charge of the gate of the external MOSFETs during PWM operation.

The flying capacitors between CPC1N/CPC1P and CPC2N/CPC2P must be as close as possible to the TLE92104-232.

The decoupling capacitors between VS/GND and VDD/GND must be as close as possible to the TLE92104-232 and short PCB tracks to the GND plane.

A resistor (RCSOx) and a capacitor (CCSOx) can be placed (not mandatory) at the output of the current sense amplifiers.

Application information

The device does not need any resistor at the output of the current sense amplifiers. However, if a resistor is used by the application, RCSOx must be higher than 1 kΩ. This resistor causes additional current consumption from VDD, which is not taken into account in the electrical characteristics of the datasheet.

CCSOx must be between 10 pF and 400 pF. For a fast reaction time of the CSA output, it is recommended to keep CCSOx to 10 pF.

If a filter is used at the inputs of the current sense amplifier, the serial resistor may not exceed 5 Ω.

It is possible that the MOSFET gate voltage goes below the source voltage during the commutation of a half-bridge. This depends on the stray inductances at the drain and the source of the MOSFET, the speed of the commutation and the ratio between the MOSFET Gate-Source and Gate-Drain capacitances.

If V_{GATE} - V_{SOURCE} < -0.6 V, a series resistor (e.g. 4.7 Ω) in series to GHx and GLx are recommended to limit current delivered by the gate driver during the commutation.

Shunt resistor in the motor phase

When the shunt resistor is placed in the motor phase, it is highly recommended to apply the PWM to the half-bridge which is not connected to the shunt resistor (**Figure 51**). This avoids a high common mode swing at the inputs of the current sense amplifier.

The drain-source monitoring of the monitoring of the drain-source overvoltage of the high-side MOSFETs must be set to DH - VSHx. Refer to **VDS1**, HBxD bits.

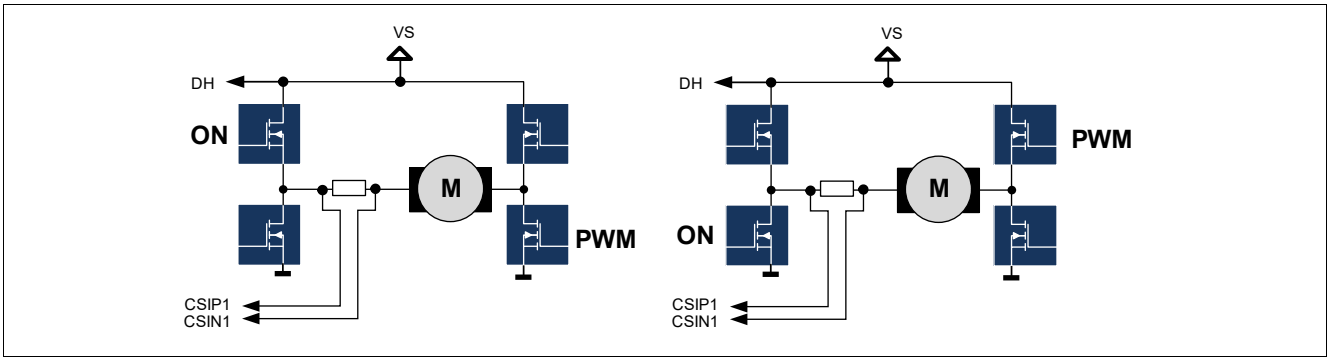


Figure 51 PWM with Shunt resistance in the motor phase

For a proper off-state diagnostic for with the shunt resistor in the motor phase, the corresponding current sense amplifier (CSA) must be deactivated. Otherwise, the activated CSA draws current from its inputs, preventing the internal pull-up source to set the SHx pin to high.

11 Package outlines

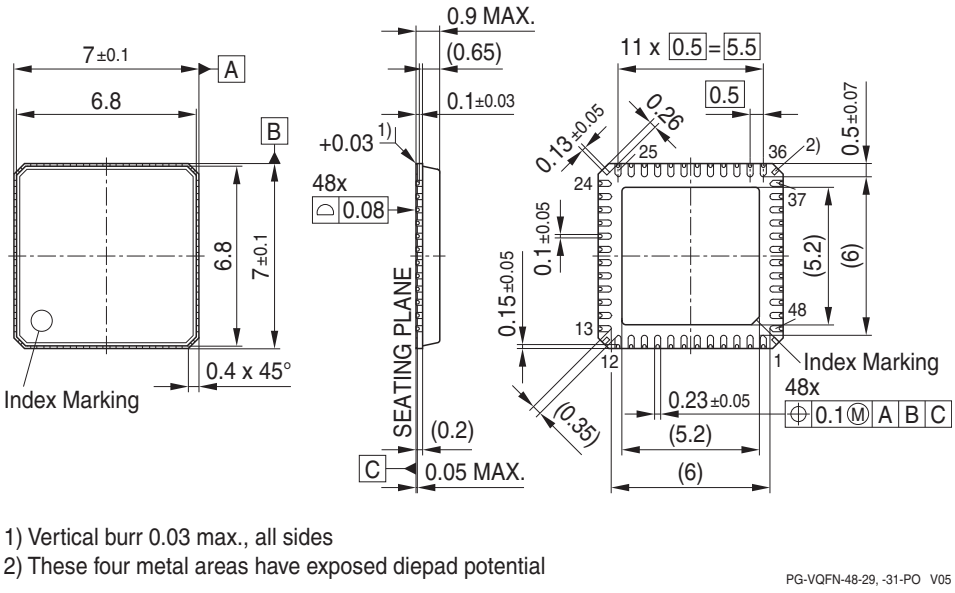


Figure 52 PG-VQFN-48[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

1) Dimmensions in mm

12 Revision History

Revision	Date	Changes
1.0	2020-09-21	First release

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